



Compal Confidential

PLA00 LA6951P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

AIO M/B

2010-11-04

REV: 0.3

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				Custom	PLA00 M/B LA-6951P Schematic
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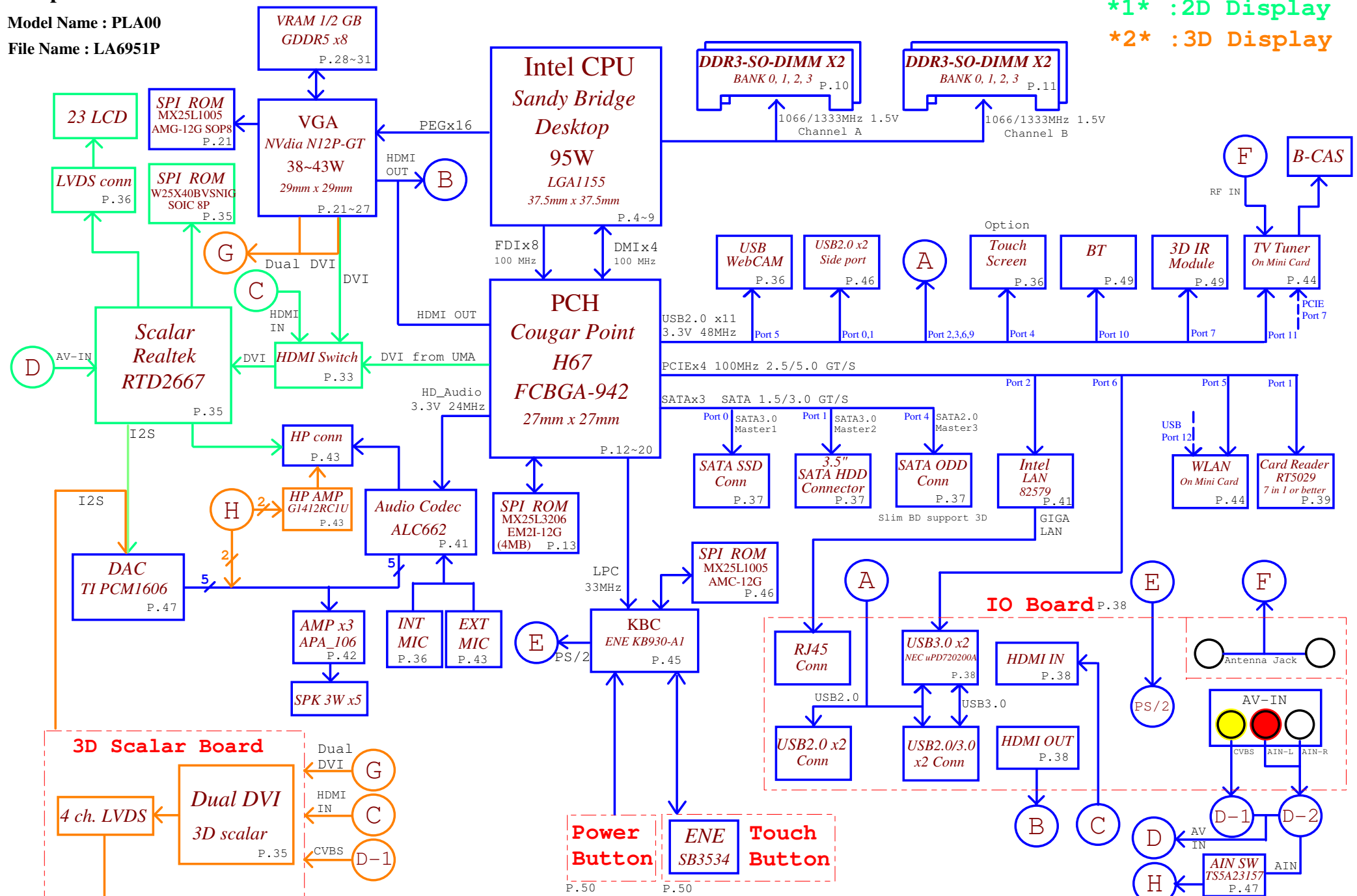
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Model Name : PLA00

File Name : LA6951P

1 :2D Display

2 :3D Display



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Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	N/A	N/A	N/A
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	OFF	ON	OFF

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID(Project) Table

Project_ID2 (GPIO38)	Project_ID1 (GPIO37)	Project_ID0 (GPIO36)	SKU
0	0	0	UMA@
0	0	1	DIS@ (VRAM:Hynix)
0	1	0	DIS@ (VRAM:Samsung)
0	1	1	X
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

EC SM Bus address

Device	Address
VGA Thermal Sensor(Internal)	0*9E H
VGA Thermal Sensor(External)	0*9A H

PCH SM Bus address

Device	Address
DDR(JDIMM1)	1010 0000 b
DDR(JDIMM2)	1010 0010 b
DDR(JDIMM4)	1010 0100 b
DDR(JDIMM3)	1010 0110 b

USB Port Table

USB 2.0	USB 1.1	Port	6 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB Conn
	UHCI1	2	USB Conn
		3	USB Conn
	UHCI2	4	Touch Screen
		5	Web Camera
EHCI2	UHCI3	6	USB 2.0
		7	3D IR
	UHCI4	8	
		9	USB 2.0
	UHCI5	10	Blue Tooth
		11	Mini Car(TV Tuner)
	UHCI6	12	Mini Car(WLAN)
		13	

BTO Option Table

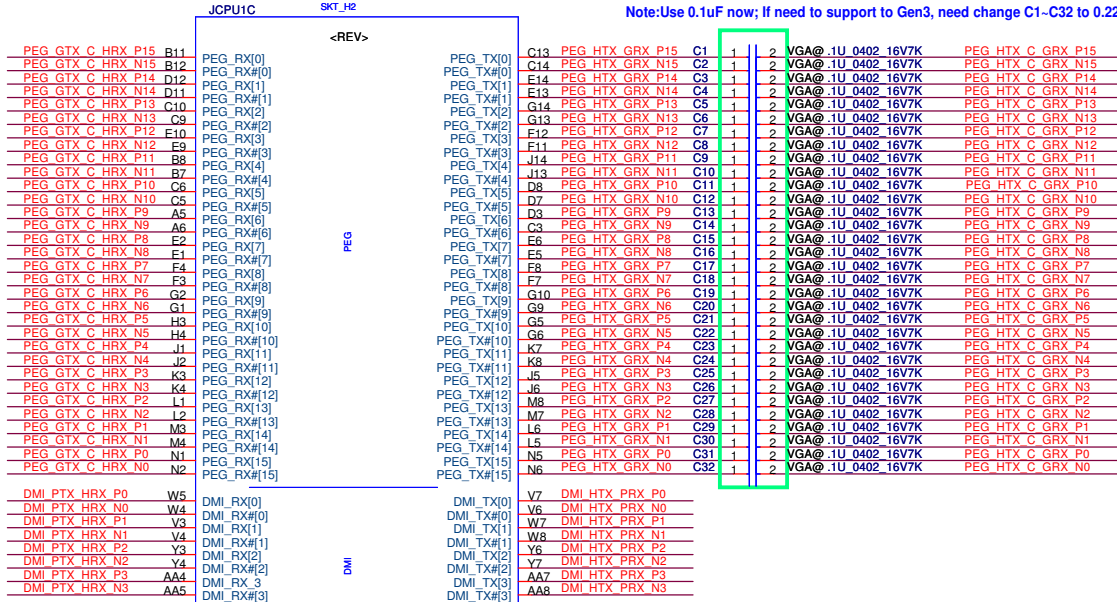
BTO Item	BOM Structure
VGA	VGA@
UMA Only	UMA@
DIS Only	DIS@
2D	2D@
3D	3D@
VGA_2D	VGA_2D@
TAS3208	3208@
PCM1606	1606@
Samsung VRAM	X76_SAM@
Hynix VRAM	X76_HYN@
CRT	CRT@

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DMI_PTX_HRX_N[0..3] <14>
DMI_PTX_HRX_P[0..3] <14>
DMI_HTX_PRX_N[0..3] <14>
DMI_HTX_PRX_P[0..3] <14>

PEG GTX_C_HRX_P[0..15] <22>
PEG GTX_C_HRX_N[0..15] <22>
PEG HTX_C_GRX_P[0..15] <22>
PEG HTX_C_GRX_N[0..15] <22>

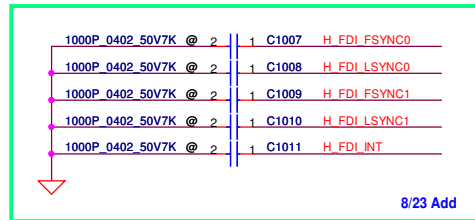
Note: Use 0.1uF now; If need to support to Gen3, need change C1~C32 to 0.22uF.



7/20 PE_RX[0-3]/PE_RX#[0-3] only use on Workstation.

7/20 PE_TX[0-3]/PE_TX#[0-3] only use on Workstation.

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - ; Width/Space= (4 mils/15mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils
- Width/Space (12 mils/15mils)



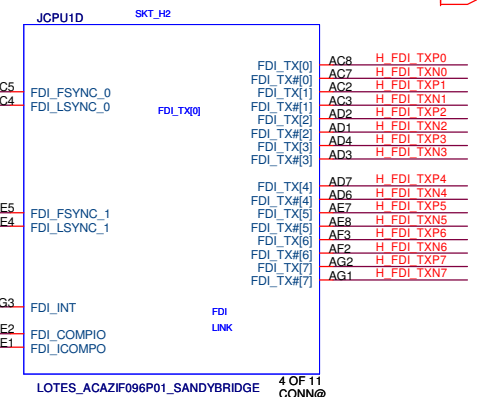
8/23 Add

H_FDI_TXN[0..7] <16>
H_FDI_TXP[0..7] <16>

<16> H_FDI_FSYNC0
<16> H_FDI_LSYNC0

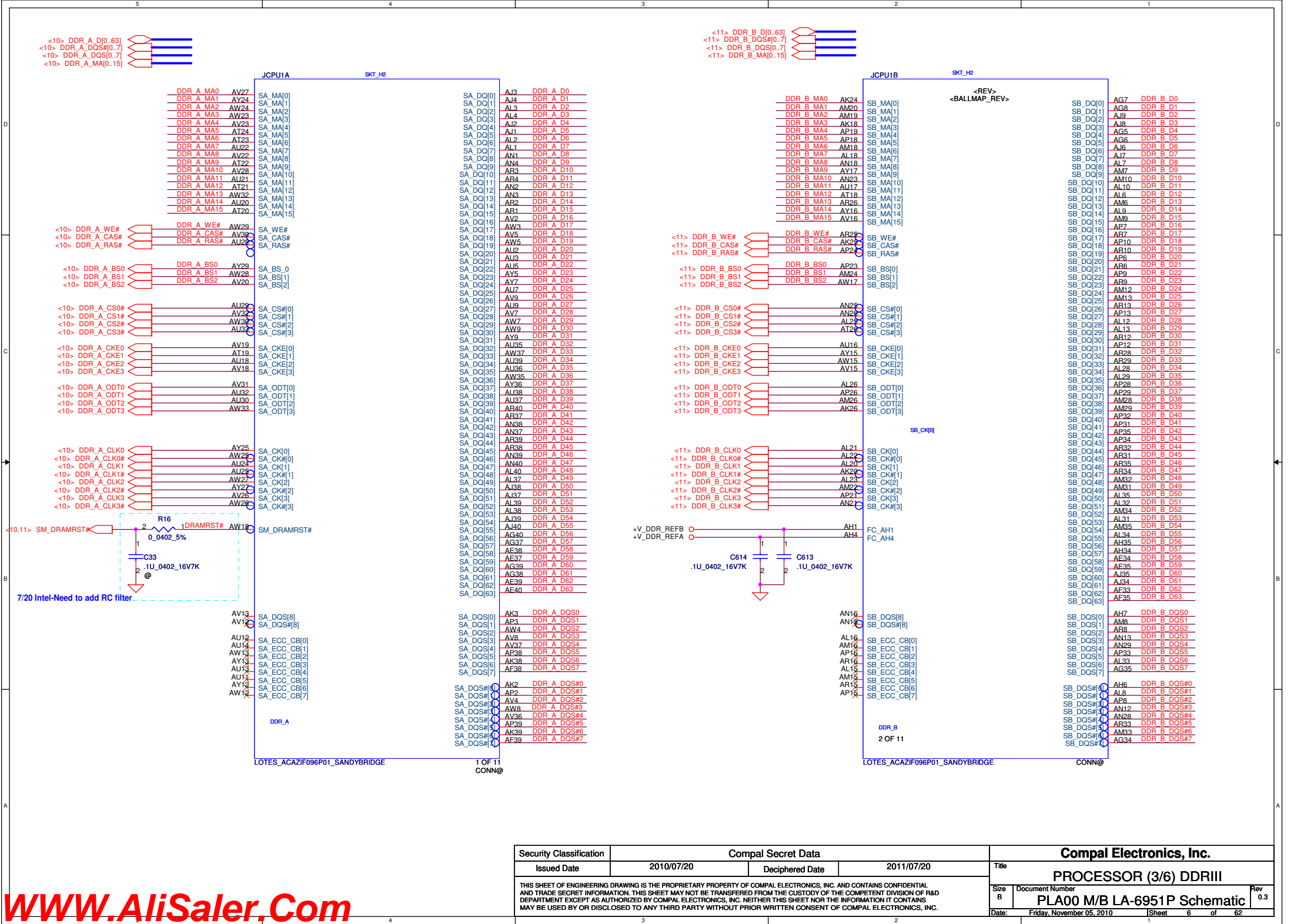
<16> H_FDI_FSYNC1
<16> H_FDI_LSYNC1

<16> H_FDI_INT
FDI_ICOMP



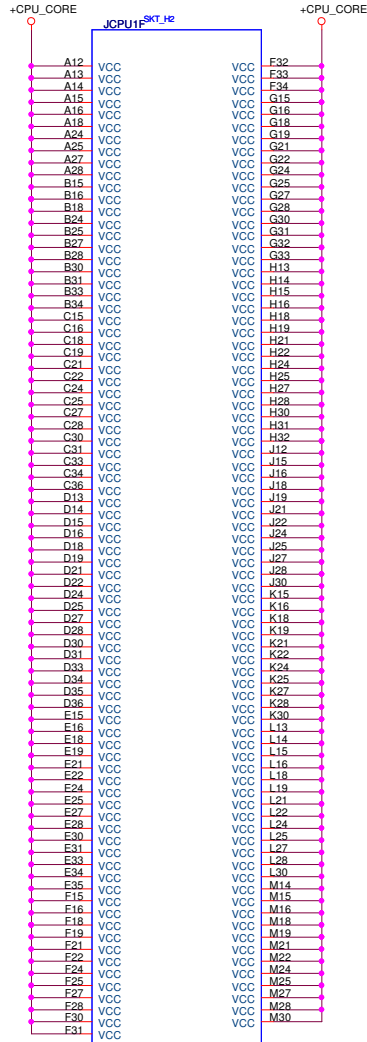
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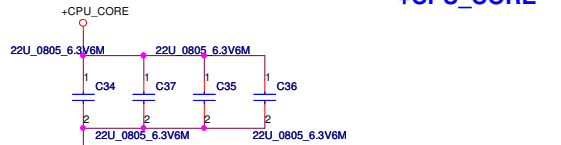
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+CPU_CORE:112A

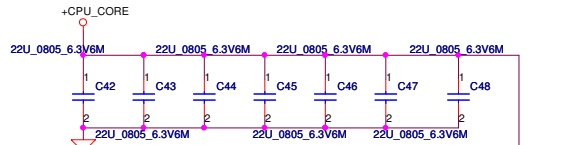


CPU POWER
6 OF 11
LOTES_ACAZIF096P01_SANDYBRIDGE
CONN@

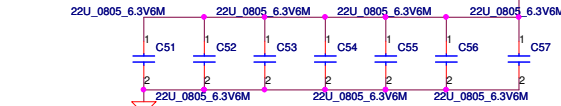
+CPU_CORE



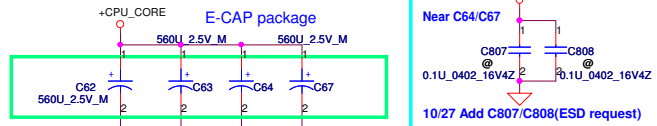
(Place these capacitors inside CPU socket cavity, top layer)



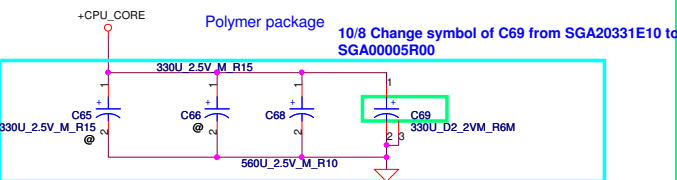
(Place these capacitors under CPU socket, Bottom layer)



(Place these capacitors under CPU socket, Bottom layer)

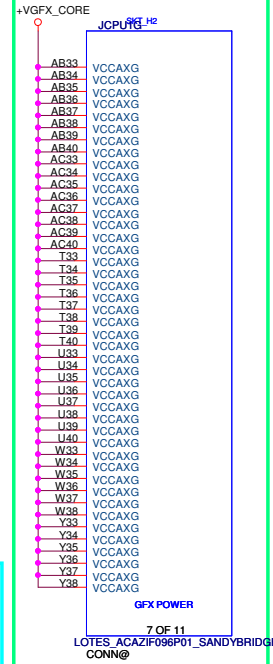


8/24 Change symbol of C62-C63 from SF000001P00 to SF000001K00
(Place C62-C64 capacitors under CPU socket, Top layer)



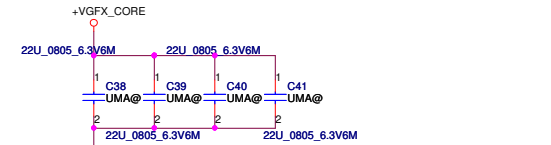
10/23 Change symbol of C65/C66/C68 from SGA20331E10 to SF000002M00
(Place C65-C69 capacitors under CPU socket, Bottom layer)
11/2 Change PN of C68 from SF000002M00 to SF000001K00

+VGFX_CORE:35A



GFX POWER
7 OF 11
LOTES_ACAZIF096P01_SANDYBRIDGE
CONN@

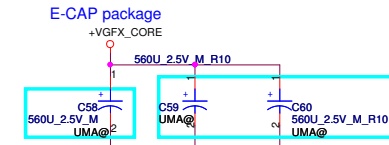
+VGFX_CORE



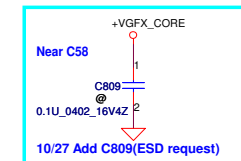
(Place these capacitors inside CPU socket cavity, top layer)



(Place these capacitors under CPU socket, Bottom layer)

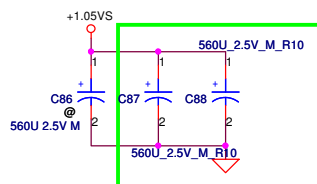
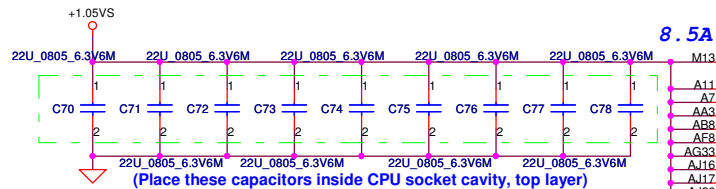


(Place C58 capacitors under CPU socket, Top layer)
(Place C59/C60 capacitors under CPU socket, Bottom layer)
8/24 Change symbol of C58 from SF000001P00 to SF000001K00
10/23 Change symbol of C59/C60 from SGA20331E10 to SF000002M00
11/2 Change PN of C59/C60 from SF000002M00 to SF000001K00



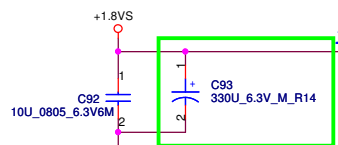
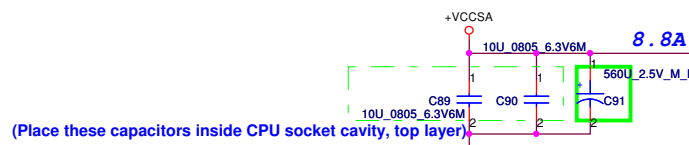
10/27 Add C89(ESD request)

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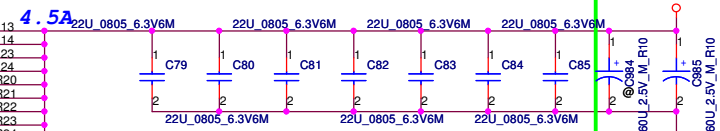
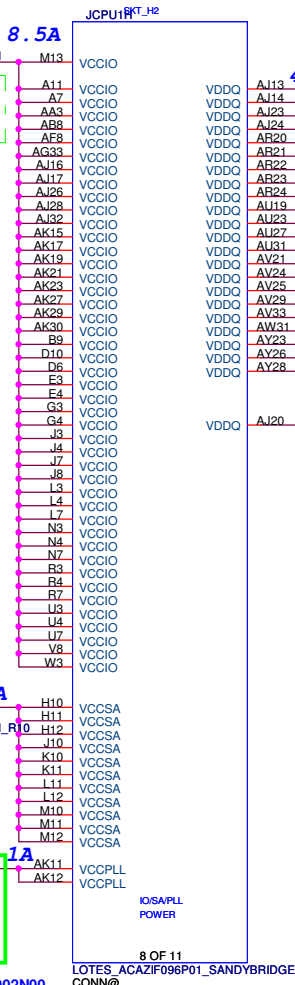


11/2 Change PN of C87/C88 from SF000001P00 to SF000001K00

11/4 Change PN of C91 from SF000001P00 to SF000001K00

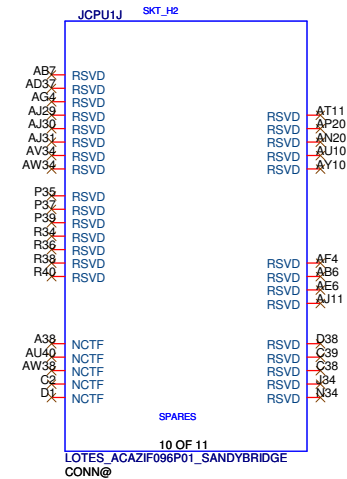
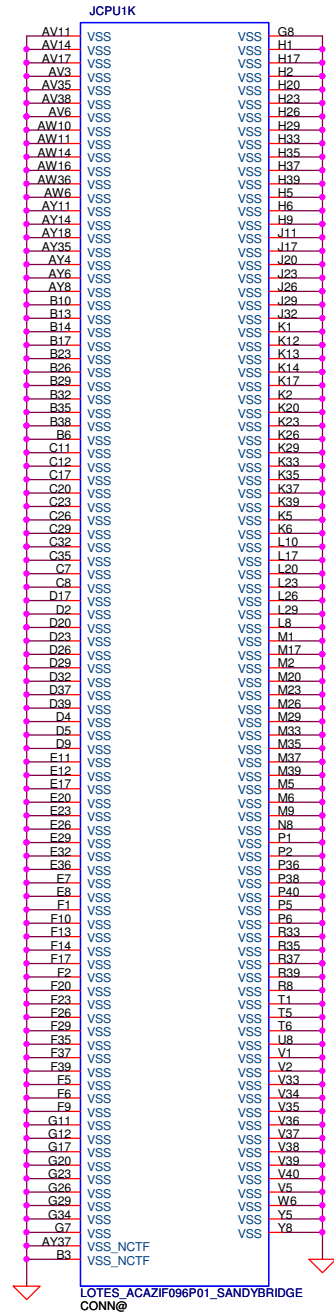
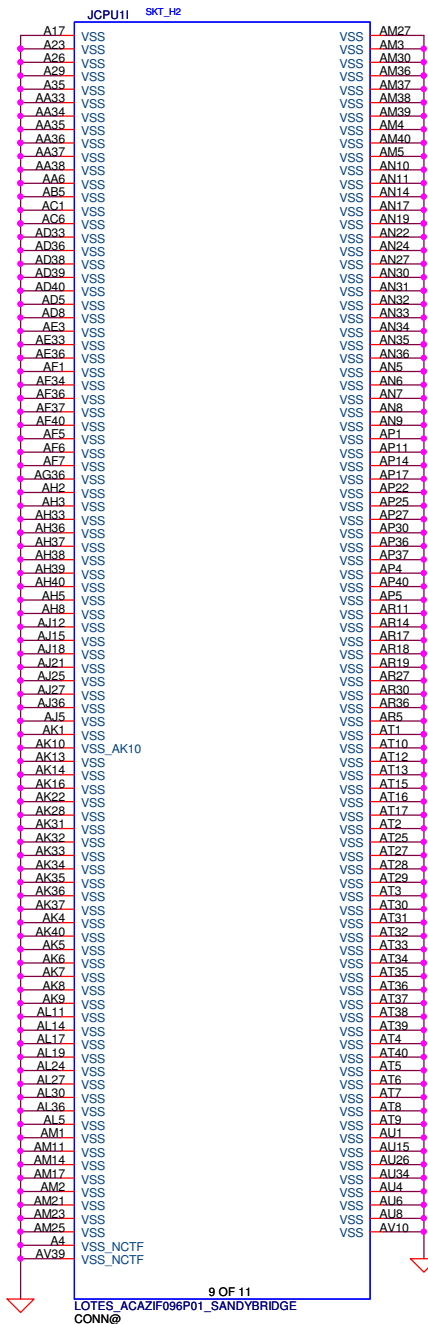


11/4 Change PN of C93 from SF000002N00 to SF000001G00



11/2 Change PN of C984/C985 from SF000002000 to SF000001K00

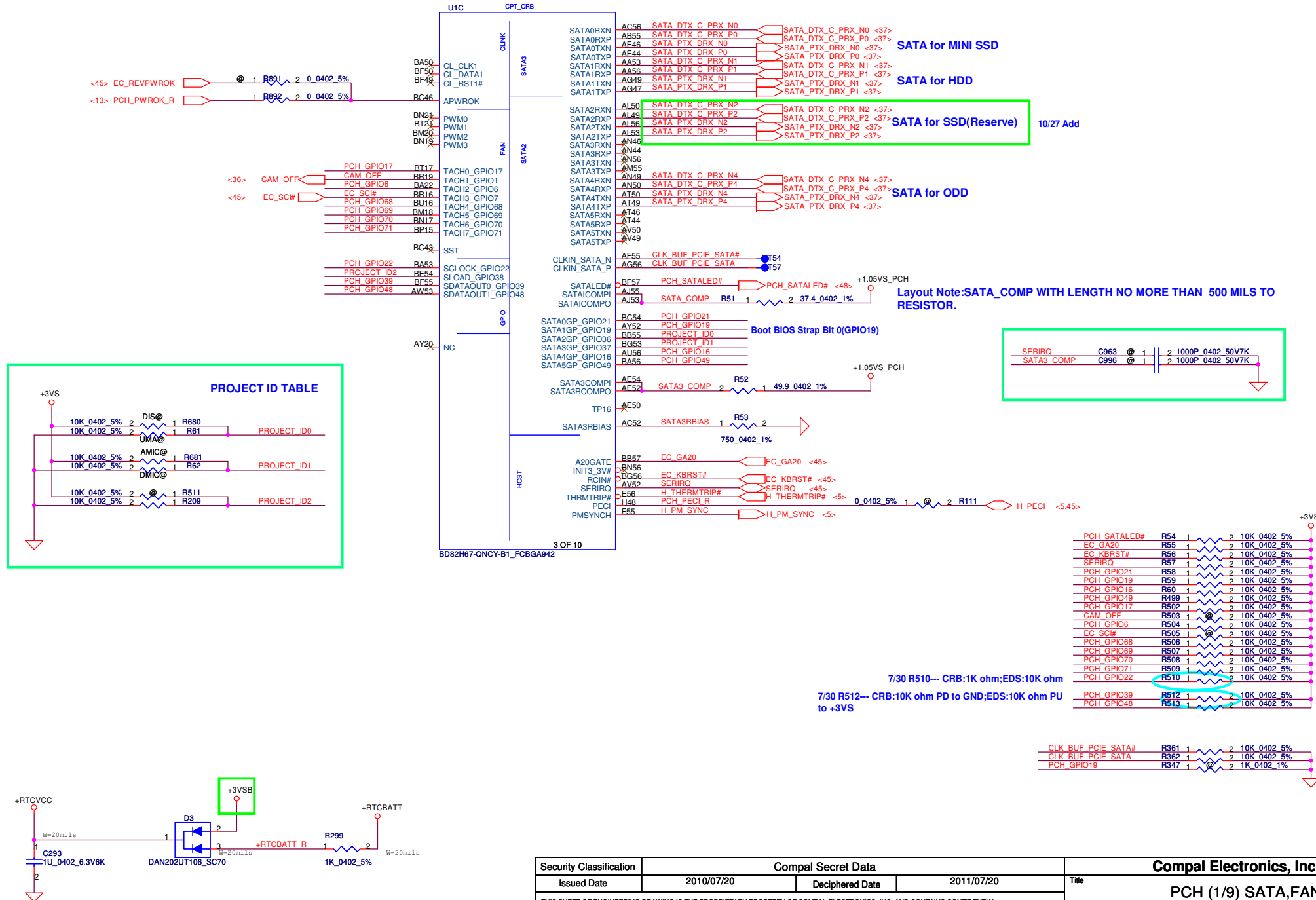
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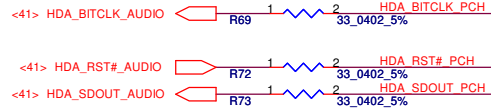
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HDA for AUDIO

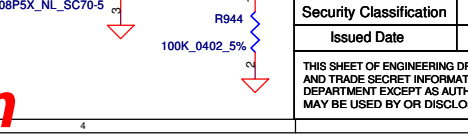
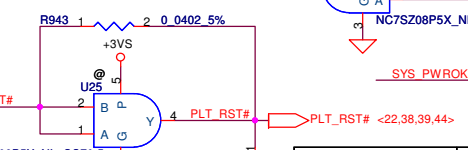
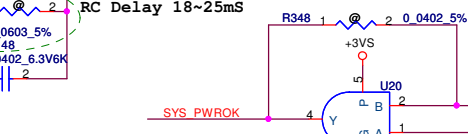
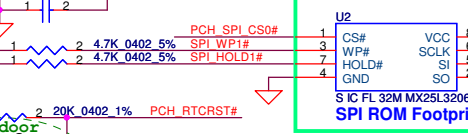
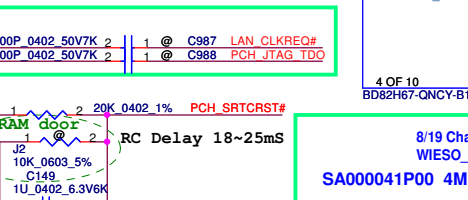
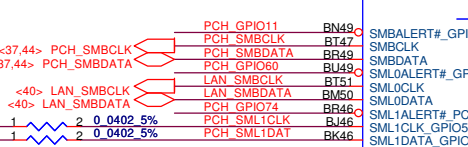
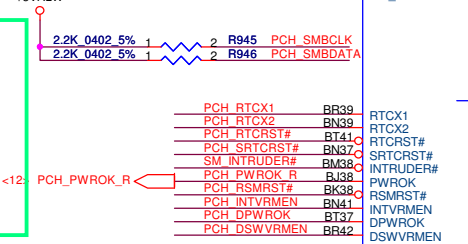
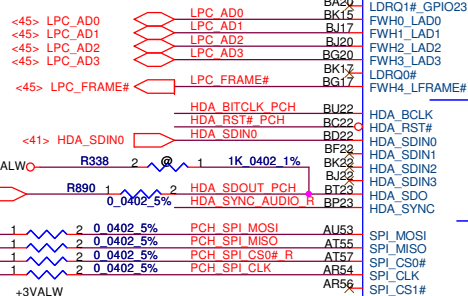
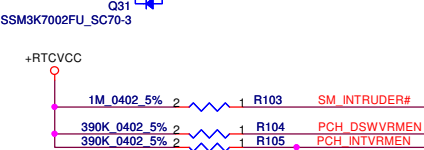
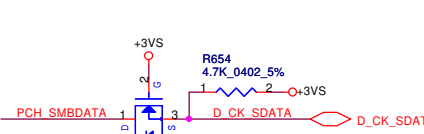
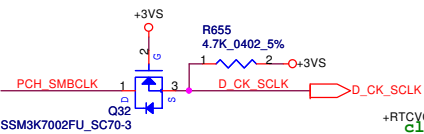
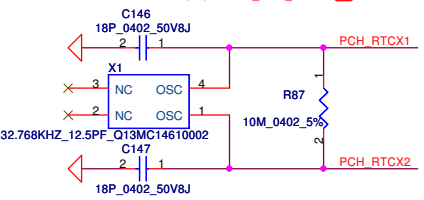
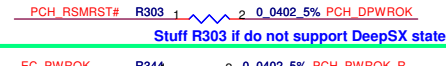
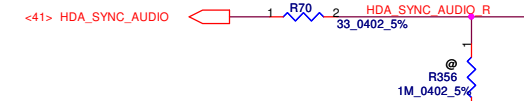


HDA_SDO

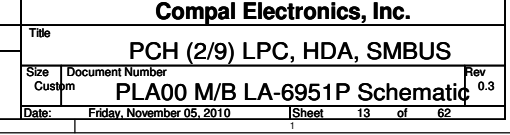
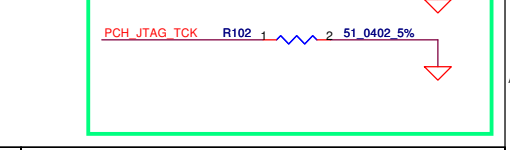
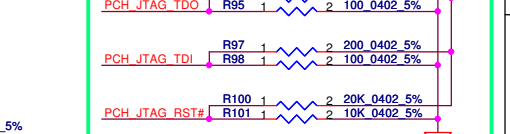
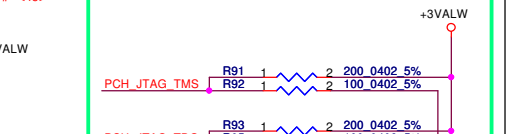
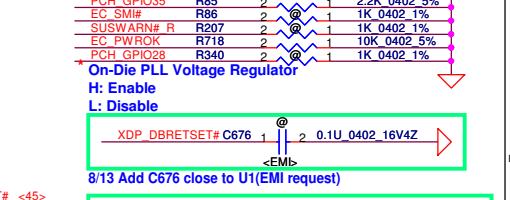
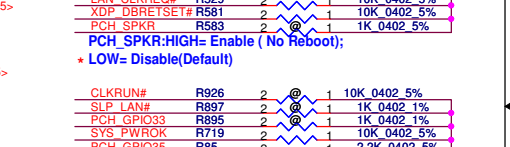
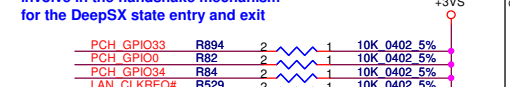
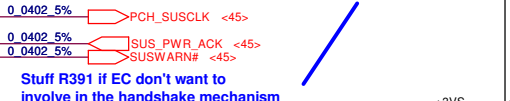
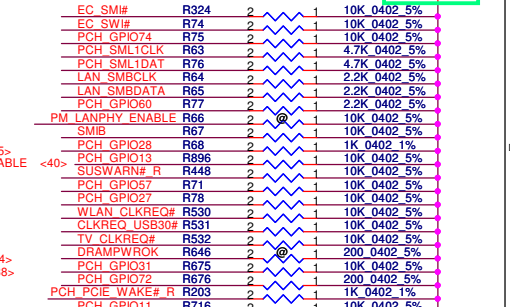
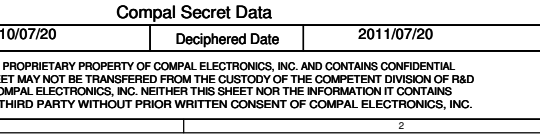
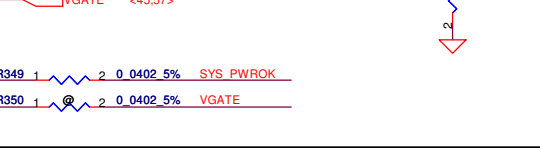
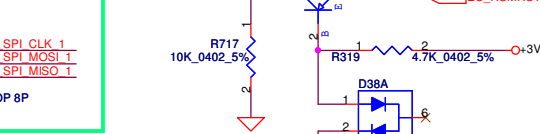
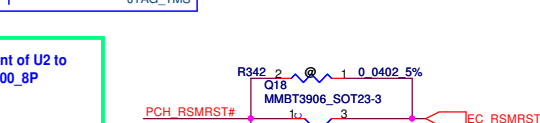
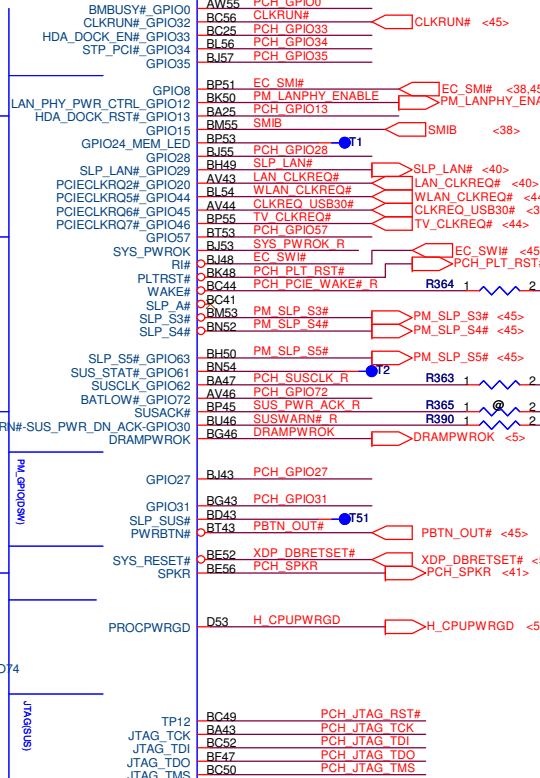
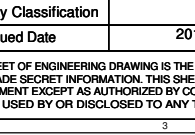
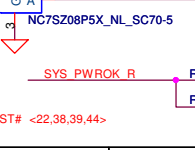
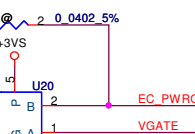
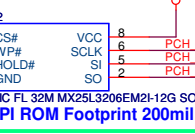
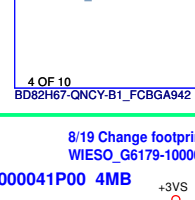
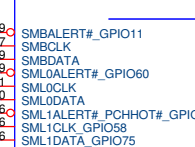
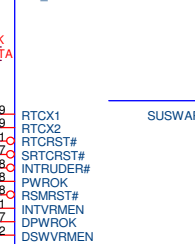
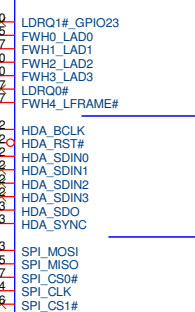
ME debug mode,
this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security override)

HDA_SYNC

This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
★Need to pull high for Huron River platform



U1D



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						Size		Document Number		Rev	
						Custom		PLA00 M/B LA-6951P Schematic		0.3	
Date:		Friday, November 05, 2010		Sheet		13		of 62			

<4> DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
<4> DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
<4> DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
<4> DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

+1.05VS_PCH
R107
49.9_0402_1%
1 2

DMI_HTX_PRX_N0 D33
DMI_HTX_PRX_P0 B33
DMI_PTX_HRX_N0 J36
DMI_HTX_PRX_N1 A36
DMI_PTX_HRX_P1 B35
DMI_HTX_PRX_N2 B38
DMI_PTX_HRX_P2 B37
DMI_HTX_PRX_N3 E37
DMI_PTX_HRX_P3 F38
DMI_HTX_PRX_N4 M41
DMI_PTX_HRX_P4 P41
DMI_HTX_PRX_N5 E31
DMI_PTX_HRX_P5 F31

DMI_COMP E31
CLK_BUF_CPU_DMI# P33
CLK_BUF_CPU_DMI R33

PCIE_DTX_C_PRX_N1 J20
PCIE_PTX_DRX_N1 L20
PCIE_DTX_C_PRX_P1 F25
PCIE_PTX_DRX_P1 F23
PCIE_DTX_C_PRX_N2 P20
PCIE_PTX_DRX_N2 P20
PCIE_DTX_C_PRX_P2 Q22
PCIE_PTX_DRX_P2 A22

H12 PETP2
J12 PERP3
E21 PETN3
B21 PETP3
P12 PERP4
M12 PERP4
F18 PETN4
E12 PETP4

PCIE_DTX_C_PRX_N5 N15
PCIE_PTX_DRX_N5 M15
PCIE_DTX_C_PRX_P5 B17
PCIE_PTX_DRX_P5 C16
PCIE_DTX_C_PRX_N6 J15
PCIE_PTX_DRX_N6 A16
PCIE_DTX_C_PRX_P6 B15
PCIE_PTX_DRX_P6 B15
PCIE_DTX_C_PRX_N7 J12
PCIE_PTX_DRX_N7 H12
PCIE_DTX_C_PRX_P7 F15
PCIE_PTX_DRX_P7 F13

H10 PERP8
J10 PERP8
B13 PETN8
D13 PETP8

U1B CPT_CRB
DMI DMI0RXN DMI0RXP DMI0TXN DMI0TXP DMI1RXN DMI1RXP DMI1TXN DMI1TXP DMI2RXN DMI2RXP DMI2TXN DMI2TXP DMI3RXN DMI3RXP DMI3TXN DMI3TXP DMI_IRCOMP DMI_ZCOMP
CLKIN_DMI_N CLKIN_DMI_P
PERN1 PERP1 PETN1 PETP1 PERN2 PERP2 PETN2 PETP2
H12 PETP2 J12 PERP3 E21 PETN3 B21 PETP3 P12 PERP4 M12 PERP4 F18 PETN4 E12 PETP4
PCIE PERP5 PERP5 PETN5 PETP5 PERP6 PERP6 PETN6 PETP6 PERP7 PERP7 PETN7 PETP7 PERP8 PERP8 PETN8 PETP8
2 OF 10
BD82H67-QNCY-B1_FCBGA942

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P
BF36 USB20_N0 BD36 USB20_P0 BA33 USB20_N1 BM33 USB20_N2 BM35 USB20_P2 BT33 USB20_N3 BU32 USB20_P3 BR32 USB20_N4 BT31 USB20_P4 BN29 USB20_N5 BM30 USB20_P5 BK33 USB20_N6 BU33 USB20_P6 BF31 USB20_N7 BD31 USB20_P7 BN27 USB20_N9 BR26 USB20_P9 BT27 USB20_P9 BK25 USB20_N10 BU25 USB20_P10 BJ25 USB20_N11 BK31 USB20_P11 BD27 USB20_P12 BF27 USB20_N12 BK27 USB20_P12 BJ27
BM43 USB_OC#0 BD41 USB_OC#1 BG41 USB_OC#2 R BK43 USB_OC#34 BP43 USB_OC#5 R BJ41 USB_OC#6 R BT45 USB_OC#7 R BM45 USB_OC#7 R
BP25 USB_BIAS BM25
BD38 CLK_BUF_DREF_96M# BF38 CLK_BUF_DREF_96M#
A32 DMI2RBIAS

USB Conn
USB Conn
USB Conn
USB Conn
Touch Screen
Web Camera
USB 2.0
3D IR
USB 2.0
Bluetooth
Mini Card(TV Tuner)
Mini Card(WLAN)

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

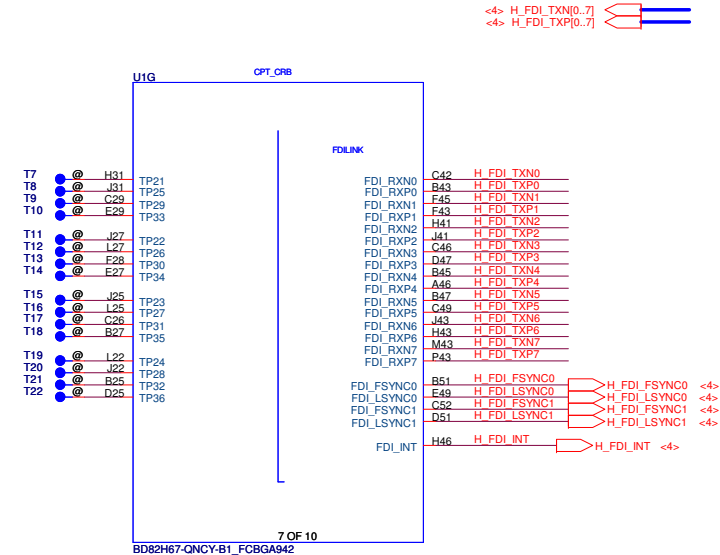
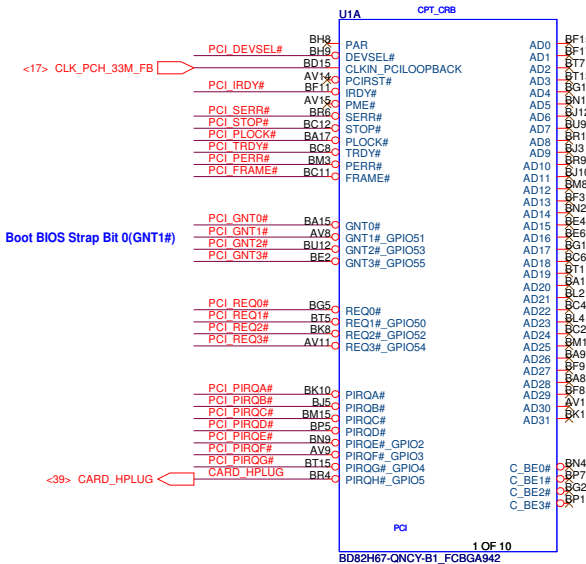
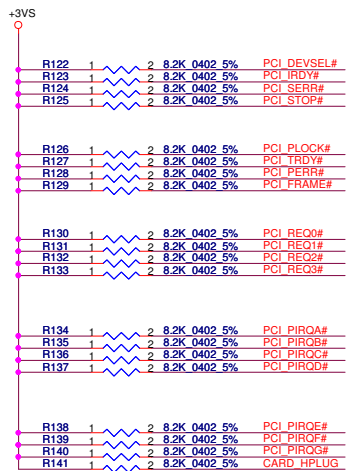
Layout Note:USB_BIAS WITH LENGTH NO MORE THAN 500 MILS TO RESISTOR.

USB_OC#2 R R110 1 2 10K 0402 5%
USB_OC#7 R R113 1 2 10K 0402 5%
USB_OC#6 R R114 1 2 10K 0402 5%
USB_OC#5 R R115 1 2 10K 0402 5%

CLK_BUF_DREF_96M# R357 1 2 10K 0402 5%
CLK_BUF_DREF_96M R358 1 2 10K 0402 5%
CLK_BUF_CPU_DMI# R359 1 2 10K 0402 5%
CLK_BUF_CPU_DMI R360 1 2 10K 0402 5%

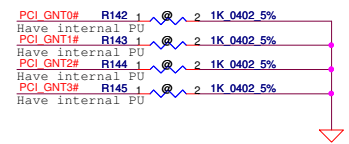
Security Classification		Compal Secret Data				Compal Electronics, Inc.											
Issued Date		2010/07/20		Deciphered Date		2011/07/20		Title									
								PCH (3/9) DMI, USB, PCIE									
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												PLA00 M/B LA-6951P Schematic					
						Date:		Friday, November 05, 2010		Sheet 14 of 62							

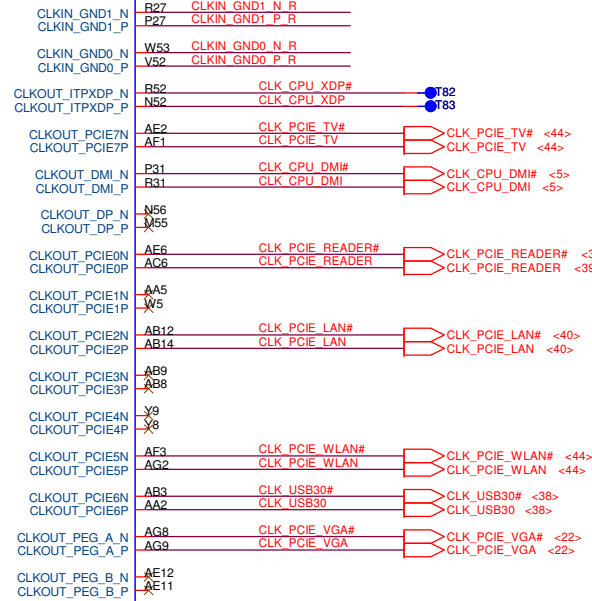
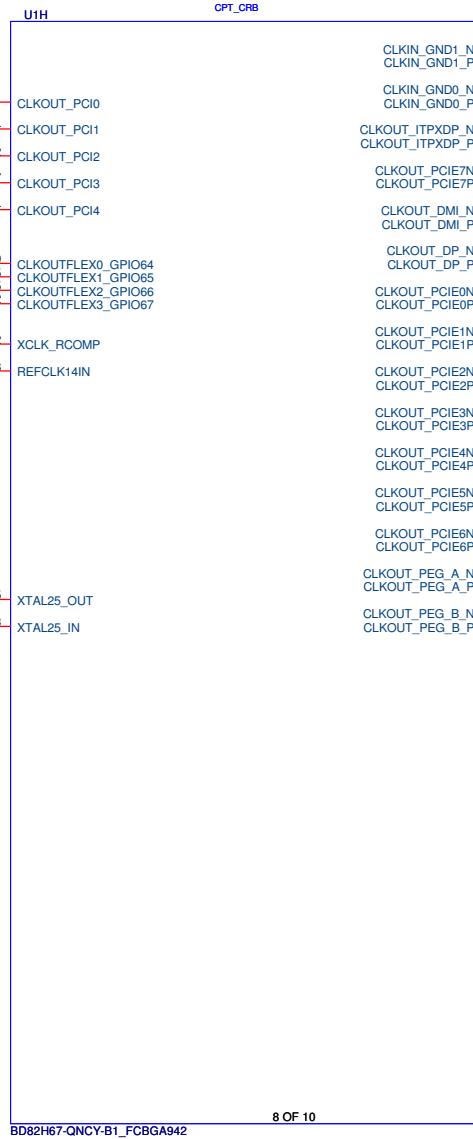
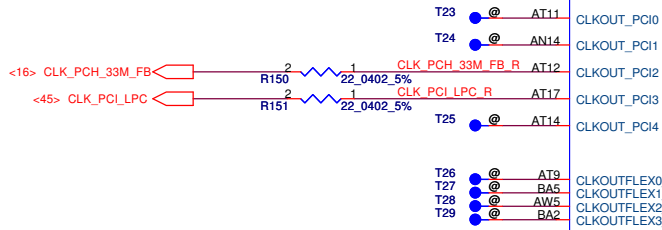
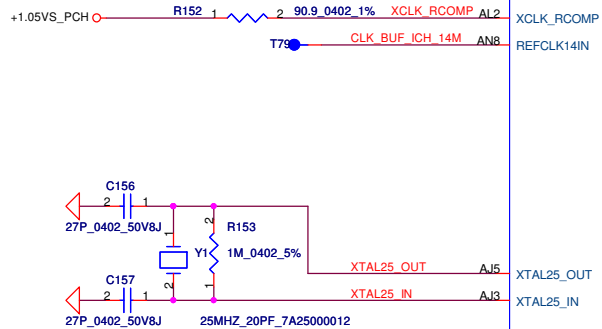




1000P_0402_50V7K 2 | 1 @ C989 CLK_PCH_33M_FB
8/23 Add

Boot BIOS Strap		
PCH_GNT1#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★





For TV Tuner

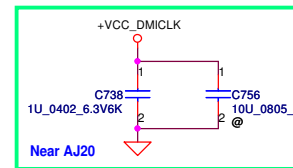
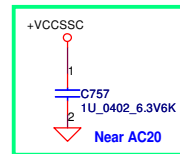
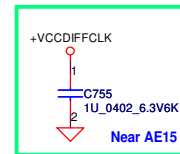
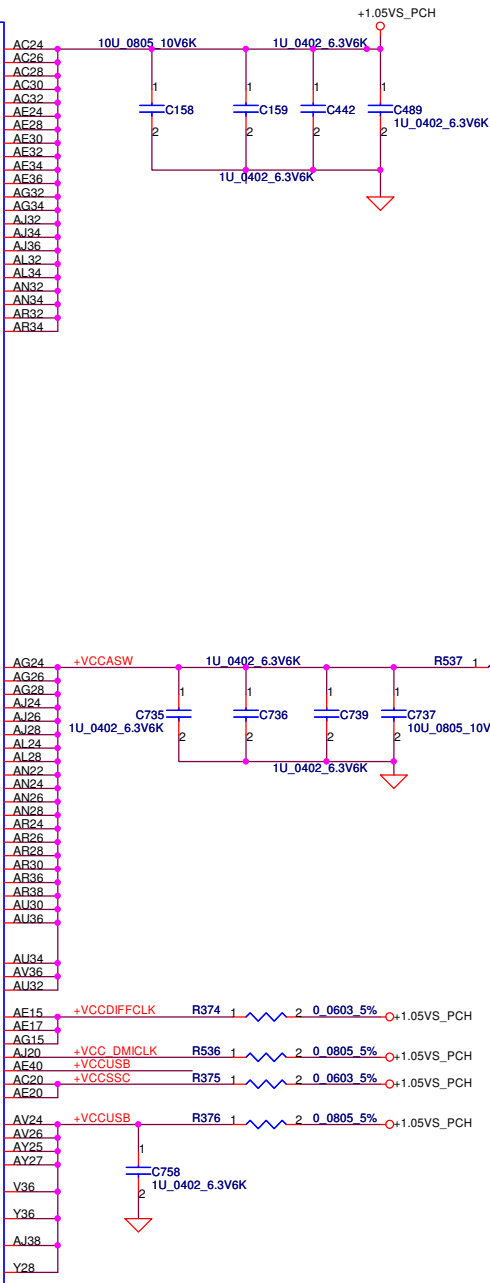
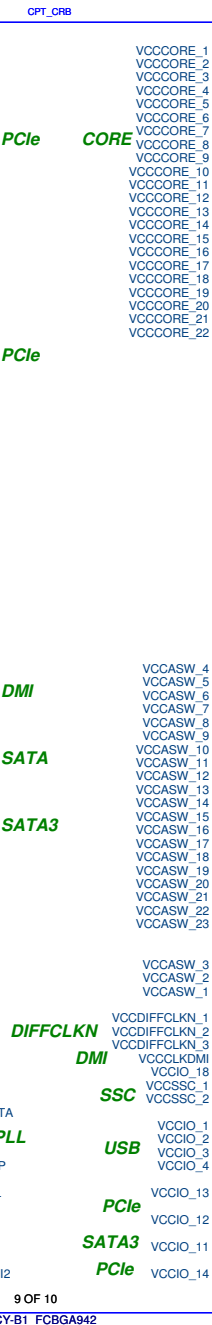
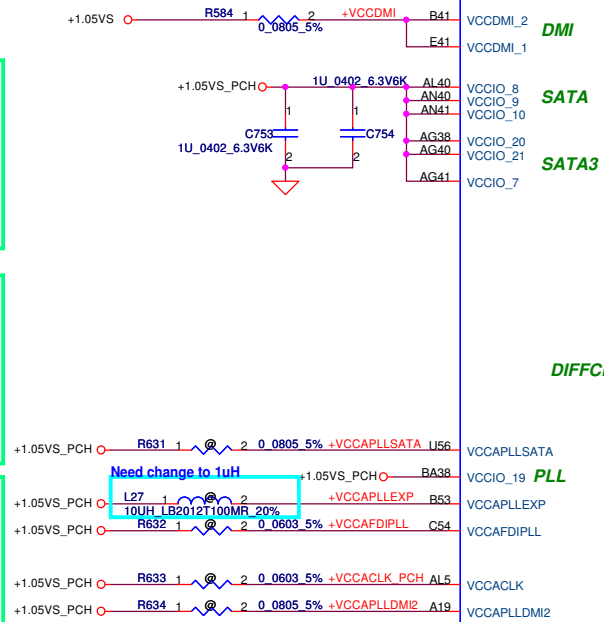
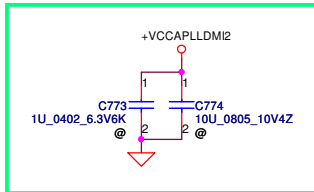
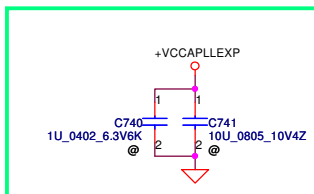
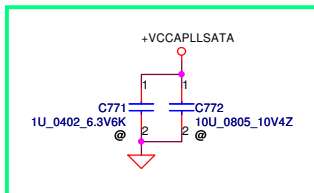
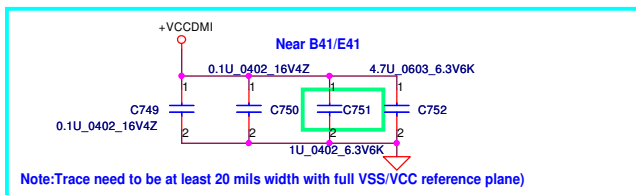
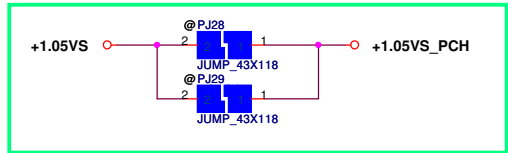
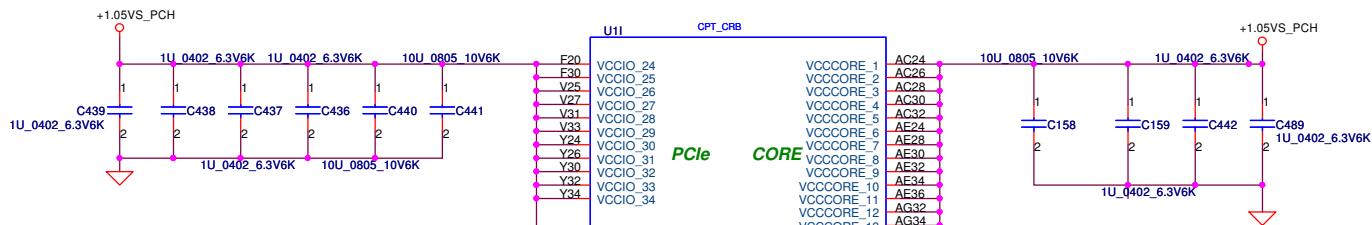
For CardReader

For PCIE LAN

For PCIE WLAN

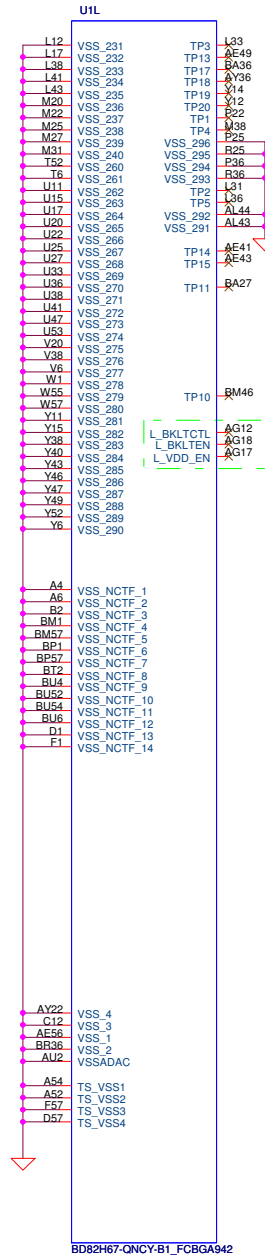
For USB 3.0

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Size	Document Number	PLA00 M/B LA-6951P Schematic		Rev	0.3
Date:	Friday, November 05, 2010	Sheet	17	of	62



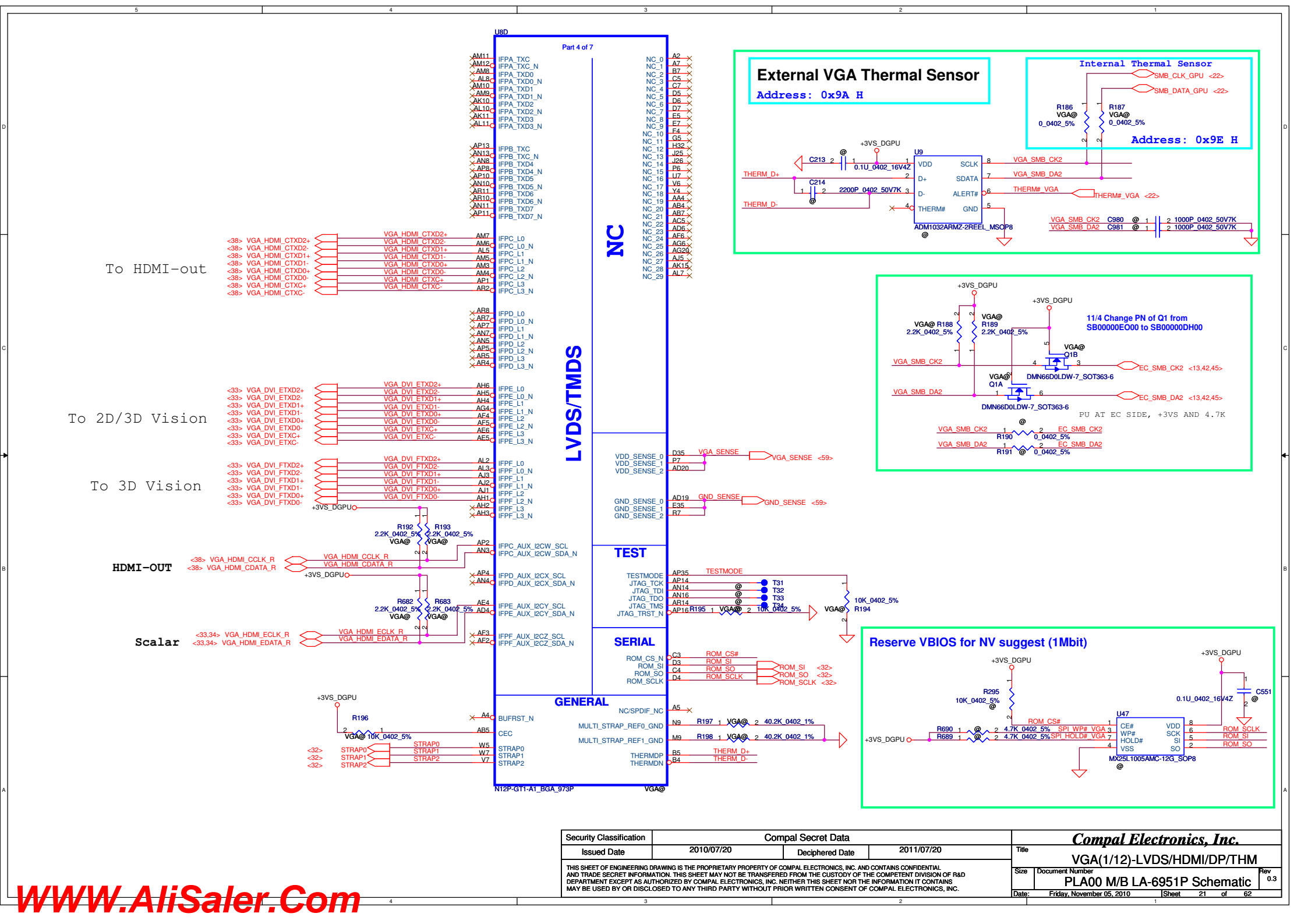
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title		
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				Size	Document Number	Rev
				Custom	PLA00 M/B LA-6951P Schematic	0.3
Date:		Friday, November 05, 2010	Sheet	18	of	62

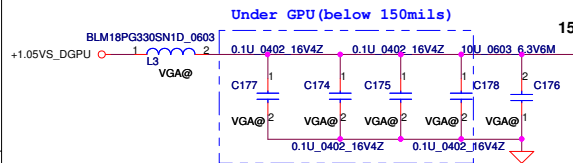
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BC15	VSS_125	VSS_5
BC20	VSS_126	VSS_6
BC27	VSS_127	VSS_7
BC31	VSS_128	VSS_8
BC38	VSS_129	VSS_9
BC47	VSS_130	VSS_10
BC9	VSS_131	VSS_11
BD25	VSS_132	VSS_12
BD33	VSS_133	VSS_13
BF12	VSS_134	VSS_14
BF20	VSS_135	VSS_15
BF25	VSS_136	VSS_16
BF33	VSS_137	VSS_17
BF41	VSS_138	VSS_18
BF43	VSS_139	VSS_19
BF46	VSS_140	VSS_20
BF52	VSS_141	VSS_21
BF6	VSS_142	VSS_22
BF6	VSS_143	VSS_23
BG22	VSS_144	VSS_24
BG25	VSS_145	VSS_25
BG27	VSS_146	VSS_26
BG31	VSS_147	VSS_27
BG33	VSS_148	VSS_28
BG36	VSS_149	VSS_29
BG38	VSS_150	VSS_30
BH52	VSS_151	VSS_31
BH6	VSS_152	VSS_32
BJ1	VSS_153	VSS_33
BJ15	VSS_154	VSS_34
BK20	VSS_155	VSS_35
BK41	VSS_156	VSS_36
BK52	VSS_157	VSS_37
BK6	VSS_158	VSS_38
BM10	VSS_159	VSS_39
BM12	VSS_160	VSS_40
BM16	VSS_161	VSS_41
BM22	VSS_162	VSS_42
BM23	VSS_163	VSS_43
BM26	VSS_164	VSS_44
BM28	VSS_165	VSS_45
BM32	VSS_166	VSS_46
BM40	VSS_167	VSS_47
BM42	VSS_168	VSS_48
BM48	VSS_169	VSS_49
BM5	VSS_170	VSS_50
BM31	VSS_171	VSS_51
BM47	VSS_172	VSS_52
BN6	VSS_173	VSS_53
BP3	VSS_174	VSS_54
BP33	VSS_175	VSS_55
BP35	VSS_176	VSS_56
BR22	VSS_177	VSS_57
BR52	VSS_178	VSS_58
BU19	VSS_179	VSS_59
BU26	VSS_180	VSS_60
BU29	VSS_181	VSS_61
BU36	VSS_182	VSS_62
BU39	VSS_183	VSS_63
C19	VSS_184	VSS_64
C32	VSS_185	VSS_65
C39	VSS_186	VSS_66
C4	VSS_187	VSS_67
D23	VSS_188	VSS_68
D3	VSS_189	VSS_69
D35	VSS_190	VSS_70
D42	VSS_191	VSS_71
D45	VSS_192	VSS_72
E19	VSS_193	VSS_73
E39	VSS_194	VSS_74
E54	VSS_195	VSS_75
E6	VSS_196	VSS_76
E9	VSS_197	VSS_77
F10	VSS_198	VSS_78
F12	VSS_199	VSS_79
F18	VSS_200	VSS_80
F22	VSS_201	VSS_81
F26	VSS_202	VSS_82
F32	VSS_203	VSS_83
F33	VSS_204	VSS_84
F35	VSS_205	VSS_85
F38	VSS_206	VSS_86
F40	VSS_207	VSS_87
F42	VSS_208	VSS_88
F46	VSS_209	VSS_89
F48	VSS_210	VSS_90
F50	VSS_211	VSS_91
F8	VSS_212	VSS_92
AV18	VSS_213	VSS_93
AV22	VSS_104	VSS_94
AV34	VSS_105	VSS_95
AV38	VSS_106	VSS_96
AV47	VSS_107	VSS_97
AV6	VSS_108	VSS_98
AW57	VSS_109	VSS_99
AY38	VSS_110	VSS_100
AY6	VSS_111	VSS_101
B23	VSS_112	VSS_102
BA11	VSS_113	VSS_103
BA12	VSS_114	VSS_104
BA31	VSS_115	VSS_105
BA41	VSS_116	VSS_106
BA44	VSS_117	VSS_107
G54	VSS_118	VSS_108
H15	VSS_119	VSS_109
H20	VSS_120	VSS_110
H22	VSS_121	VSS_111
H25	VSS_122	VSS_112
H27	VSS_123	VSS_113
H33	VSS_124	VSS_114
H6	VSS_125	VSS_115
J1	VSS_126	VSS_116
J33	VSS_127	VSS_117
J46	VSS_128	VSS_118
J48	VSS_129	VSS_119
J5	VSS_130	VSS_120
J53	VSS_131	VSS_121
K52	VSS_132	VSS_122
K6	VSS_133	VSS_123
K9	VSS_134	VSS_124
	VSS_135	VSS_125
	VSS_136	VSS_126
	VSS_137	VSS_127
	VSS_138	VSS_128
	VSS_139	VSS_129
	VSS_140	VSS_130
	VSS_141	VSS_131
	VSS_142	VSS_132
	VSS_143	VSS_133
	VSS_144	VSS_134
	VSS_145	VSS_135
	VSS_146	VSS_136
	VSS_147	VSS_137
	VSS_148	VSS_138
	VSS_149	VSS_139
	VSS_150	VSS_140
	VSS_151	VSS_141
	VSS_152	VSS_142
	VSS_153	VSS_143
	VSS_154	VSS_144
	VSS_155	VSS_145
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	VSS_162	VSS_152
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	VSS_259	VSS_249



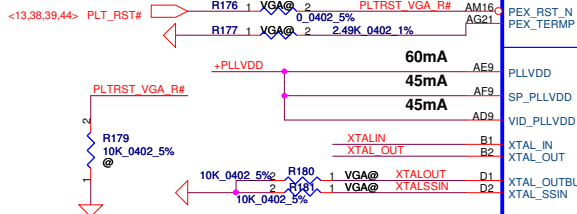
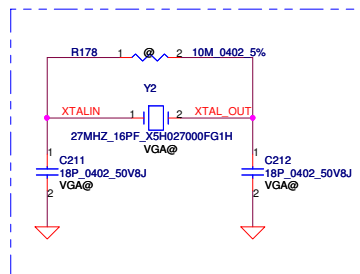
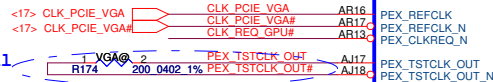
NOTE: PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCT pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

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Size	Document Number	Rev		Date	
Custom	PLA00 M/B LA-6951P Schematic	0.3		Friday, November 05, 2010	
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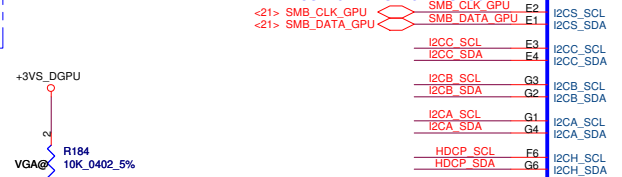




PEG GTX C HRX P0	C179	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P0	AL17
PEG GTX C HRX N0	C180	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N0	AM17
PEG GTX C HRX P1	C181	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P1	AM19
PEG GTX C HRX N1	C182	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N1	AM19
PEG GTX C HRX P2	C183	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P2	AL19
PEG GTX C HRX N2	C184	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N2	AK19
PEG GTX C HRX P3	C185	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P3	AL20
PEG GTX C HRX N3	C186	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N3	AM20
PEG GTX C HRX P4	C187	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P4	AM21
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PEG GTX C HRX P5	C189	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P5	AM22
PEG GTX C HRX N5	C190	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N5	AK22
PEG GTX C HRX P6	C191	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P6	AL23
PEG GTX C HRX N6	C192	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N6	AM23
PEG GTX C HRX P7	C193	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P7	AM24
PEG GTX C HRX N7	C194	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N7	AM25
PEG GTX C HRX P8	C195	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P8	AL25
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PEG GTX C HRX N10	C200	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N10	AM28
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PEG GTX C HRX N15	C210	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N15	AP32



Internal Thermal Sensor



PEG HTX C GRX P0	AP17
PEG HTX C GRX N0	AN17
PEG HTX C GRX P1	AP19
PEG HTX C GRX N1	AN19
PEG HTX C GRX P2	AP19
PEG HTX C GRX N2	AN19
PEG HTX C GRX P3	AP20
PEG HTX C GRX N3	AN20
PEG HTX C GRX P4	AP22
PEG HTX C GRX N4	AN22
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PEG HTX C GRX N5	AN22
PEG HTX C GRX P6	AP23
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PEG HTX C GRX P13	AN31
PEG HTX C GRX N13	AN31
PEG HTX C GRX P14	AR31
PEG HTX C GRX N14	AR32
PEG HTX C GRX P15	AR34
PEG HTX C GRX N15	AP34

Part 1 of 7

GPIO

PCI EXPRESS

DVO

CLK

I2C

DACS

GPIO

PCI EXPRESS

DVO

CLK

I2C

DACS

GPIO

PCI EXPRESS

DVO

CLK

I2C

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CLK

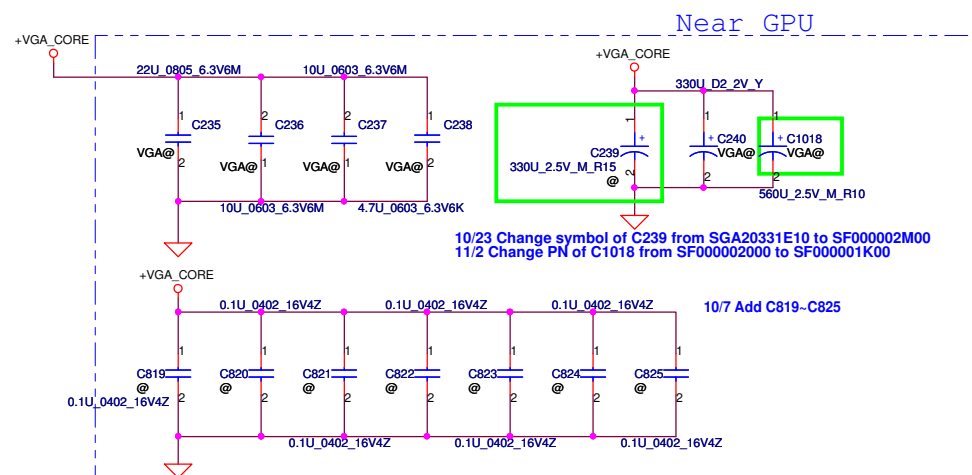
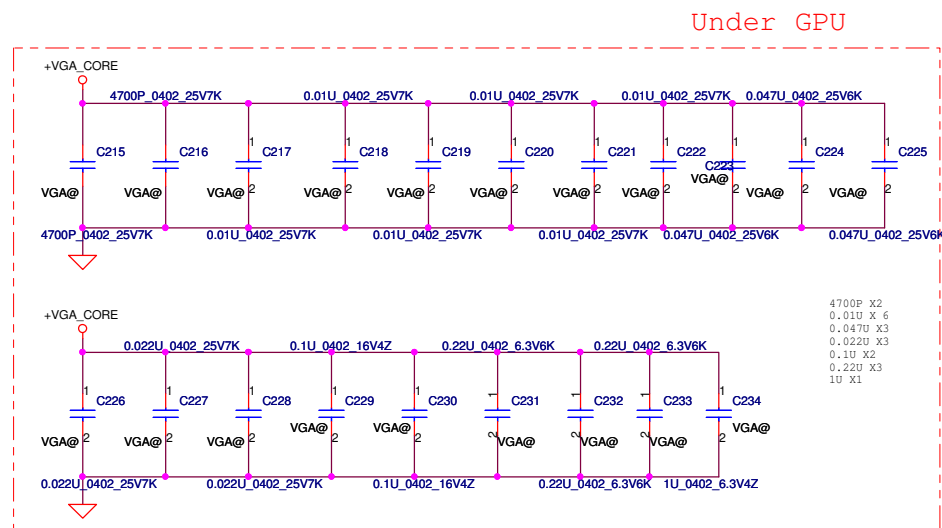
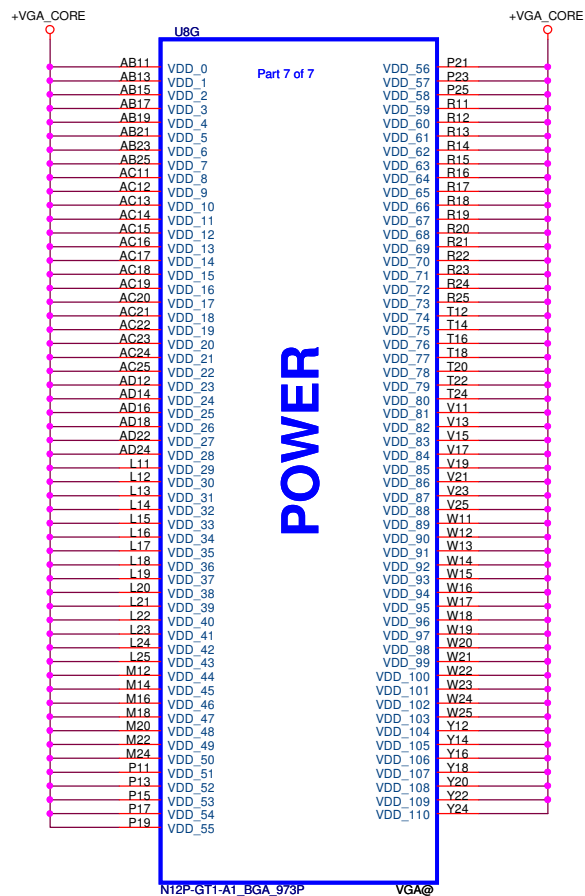
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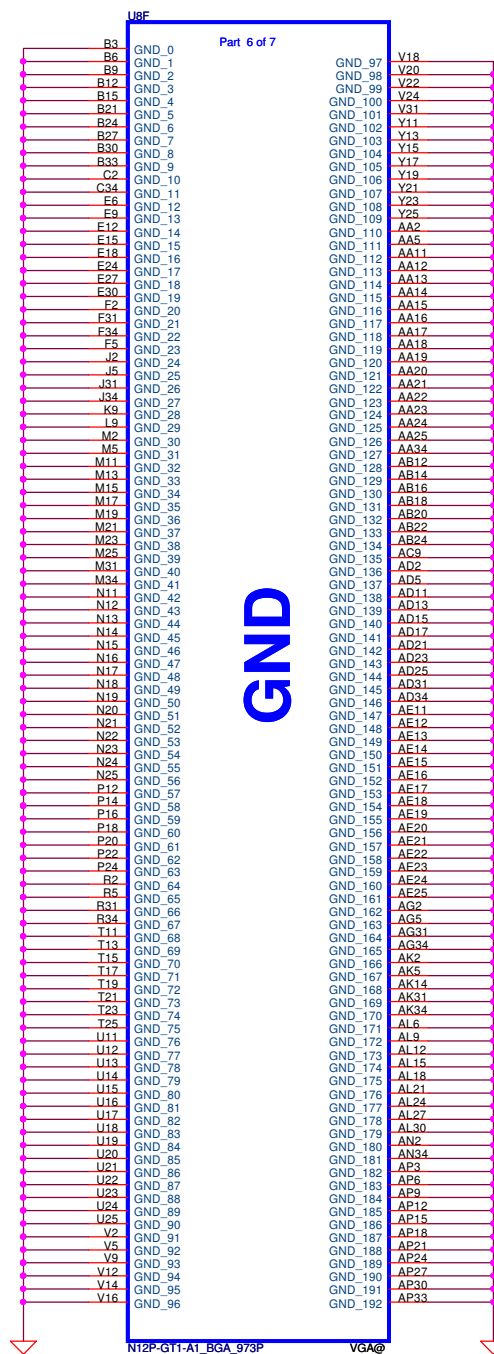
GPIO

PCI EXPRESS

DVO



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				PLA00 M/B LA-6951P Schematic	
				Date:	Thursday, November 04, 2010
				Sheet	23 of 62
				Rev	0.3



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		Size		Document Number					Rev	
		PLA00 M/B LA-6951P Schematic								0.3
		Date:		Thursday, November 04, 2010			Sheet		25	of

<30,31> MDB[0..63] ← MDB[0..63]

MDB0 B13 FBC_D0
MDB1 D13 FBC_D1
MDB2 A13 FBC_D2
MDB3 C16 FBC_D3
MDB4 C16 FBC_D4
MDB5 B16 FBC_D5
MDB6 A17 FBC_D6
MDB7 D16 FBC_D7
MDB8 C13 FBC_D8
MDB9 B11 FBC_D9
MDB10 C11 FBC_D10
MDB11 A11 FBC_D11
MDB12 C10 FBC_D12
MDB13 B8 FBC_D13
MDB14 A8 FBC_D14
MDB15 E8 FBC_D15
MDB16 F8 FBC_D16
MDB17 F12 FBC_D17
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MDB47 E29 FBC_D47
MDB48 B29 FBC_D48
MDB49 C31 FBC_D49
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MDB58 A28 FBC_D58
MDB59 C26 FBC_D59
MDB60 D25 FBC_D60
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MDB62 FBC_D62
MDB63 A25 FBC_D63

Part 3 of 7

MEMORY INTERFACE C

FBC_CMD0 E18 CMDB0
FBC_CMD1 E19 CMDB1
FBC_CMD2 D19 CMDB2
FBC_CMD3 G17 CMDB3
FBC_CMD4 F19 CMDB4
FBC_CMD5 C19 CMDB5
FBC_CMD6 B17 CMDB6
FBC_CMD7 E20 CMDB7
FBC_CMD8 B19 CMDB8
FBC_CMD9 D20 CMDB9
FBC_CMD10 A19 CMDB10
FBC_CMD11 D19 CMDB11
FBC_CMD12 C20 CMDB12
FBC_CMD13 F20 CMDB13
FBC_CMD14 B20 CMDB14
FBC_CMD15 G21 CMDB15
FBC_CMD16 F22 CMDB16
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FBC_CMD21 E22 CMDB21
FBC_CMD22 D21 CMDB22
FBC_CMD23 A23 CMDB23
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FBC_CMD25 D22 CMDB25
FBC_CMD26 B23 CMDB26
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FBC_CMD31 G20 CMDB30

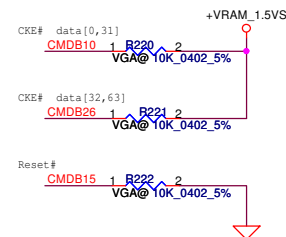
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FBC_DOM3 D27 DOMB3
FBC_DOM4 D34 DOMB4
FBC_DOM5 A34 DOMB5
FBC_DOM6 D28 DOMB6
FBC_DOM7 D28 DOMB7

FBC_DQS_RN0 B14 T43 @
FBC_DQS_RN1 B10 T44 @
FBC_DQS_RN2 D9 T45 @
FBC_DQS_RN3 E14 T46 @
FBC_DQS_RN4 F26 T47 @
FBC_DQS_RN5 A31 T48 @
FBC_DQS_RN6 A26 T49 @
FBC_DQS_RN7 A26 T50 @

FBC_DQS_WP0 C14 DQSB0
FBC_DQS_WP1 A10 DQSB1
FBC_DQS_WP2 E10 DQSB2
FBC_DQS_WP3 D14 DQSB3
FBC_DQS_WP4 E26 DQSB4
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FBC_DQS_WP6 A32 DQSB6
FBC_DQS_WP7 B26 DQSB7

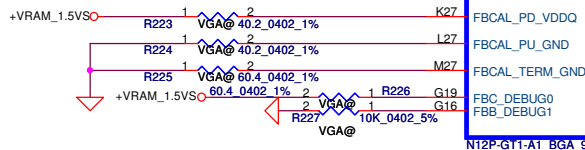
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FBC_WCK0_N G15 FBB_WCK01# FBB_WCK01# <30>
FBC_WCK1 G11 FBB_WCK23# FBB_WCK23 <30>
FBC_WCK1_N G12 FBB_WCK23# FBB_WCK23# <30>
FBC_WCK2 G27 FBB_WCK45# FBB_WCK45 <31>
FBC_WCK2_N G28 FBB_WCK45# FBB_WCK45# <31>
FBC_WCK3 G24 FBB_WCK67# FBB_WCK67 <31>
FBC_WCK3_N G25 FBB_WCK67# FBB_WCK67# <31>

FBC_CLK0 E17 CLKB0
FBC_CLK0_N D17 CLKB0#
FBC_CLK1 D23 CLKB1
FBC_CLK1_N E23 CLKB1#



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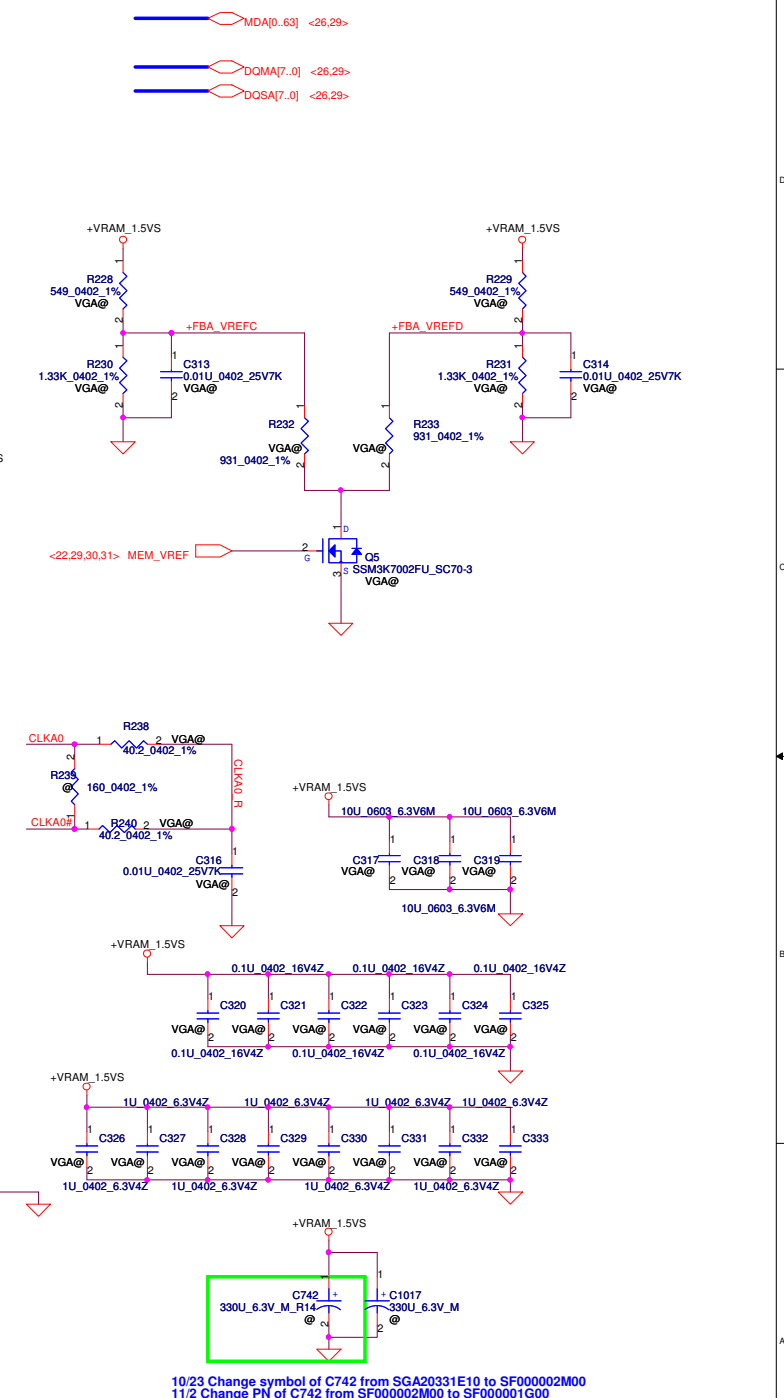
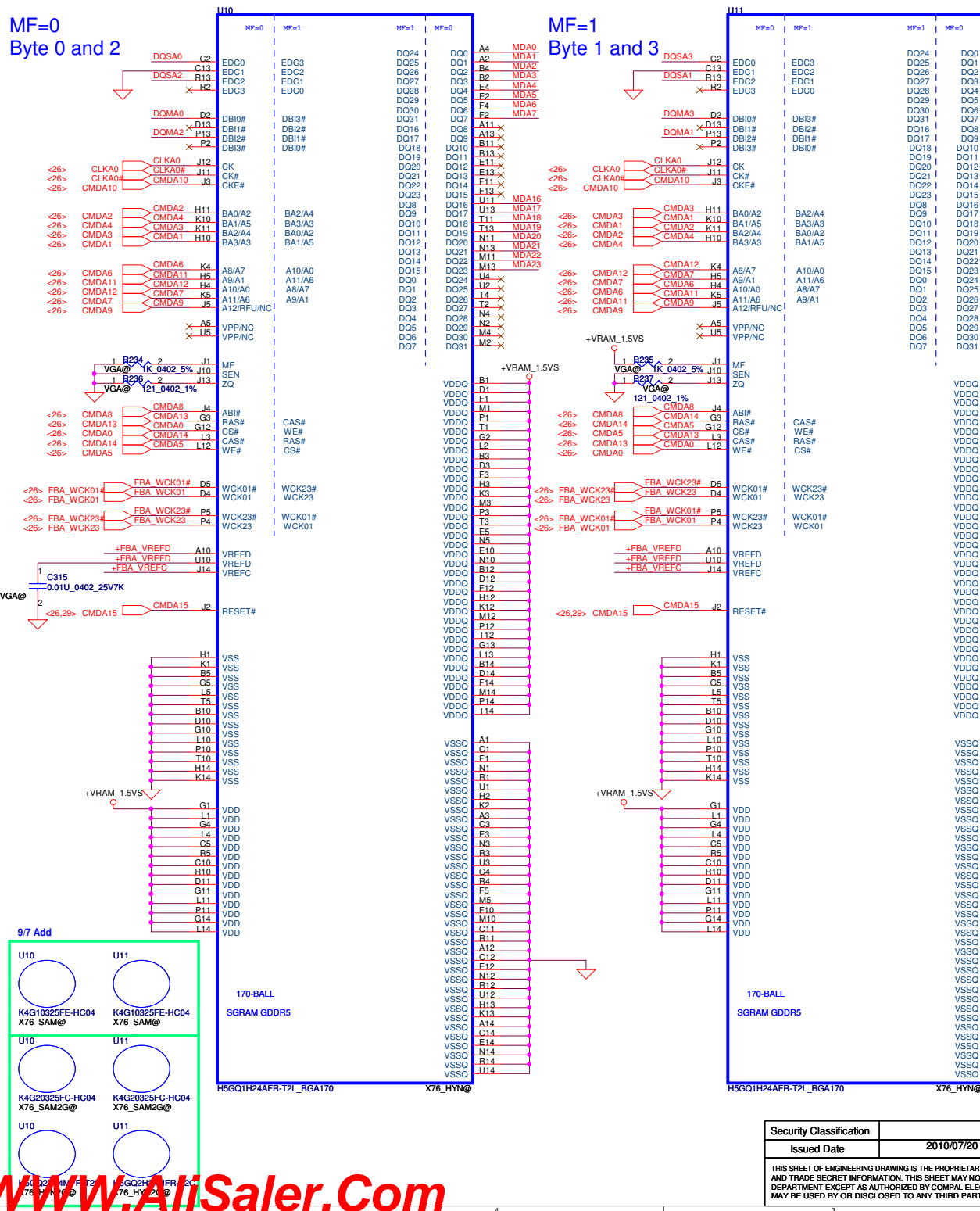
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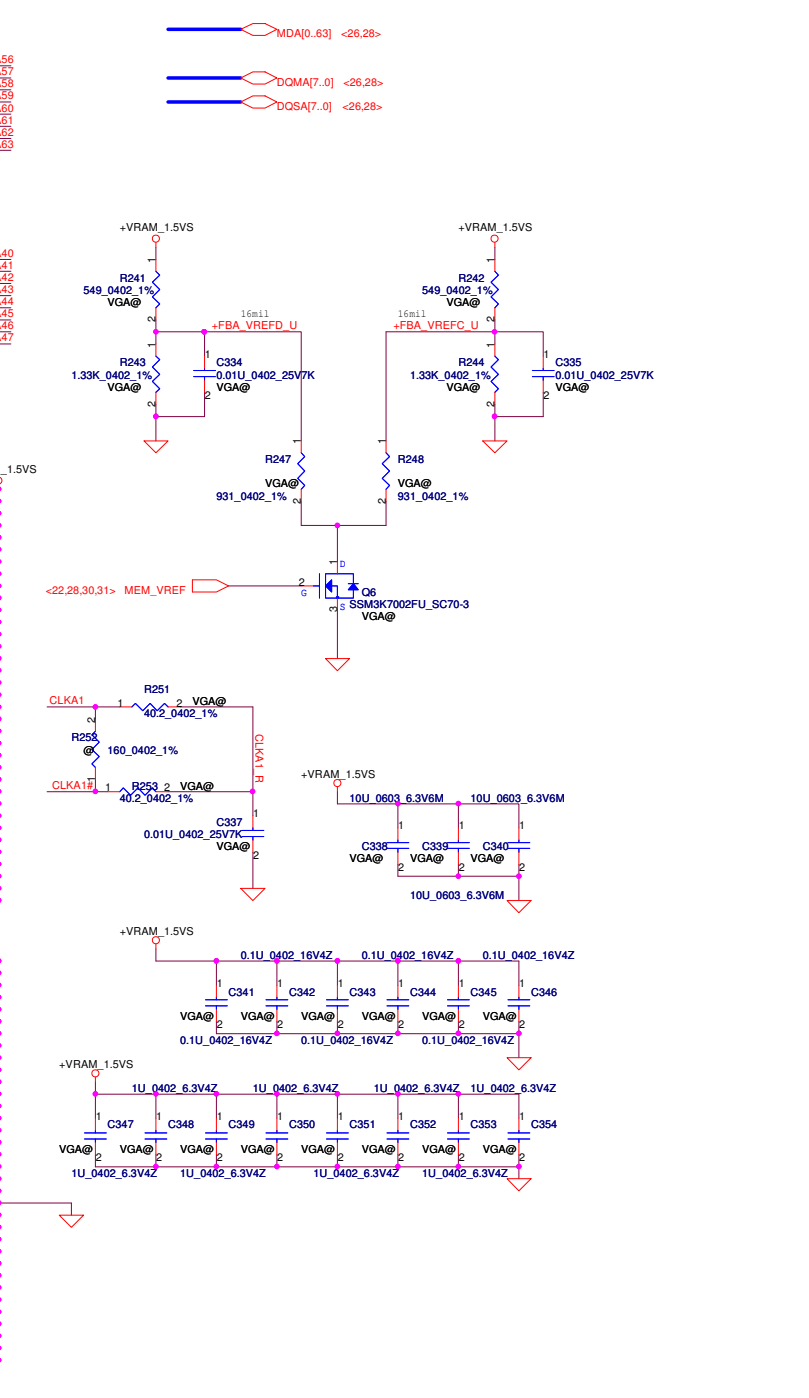
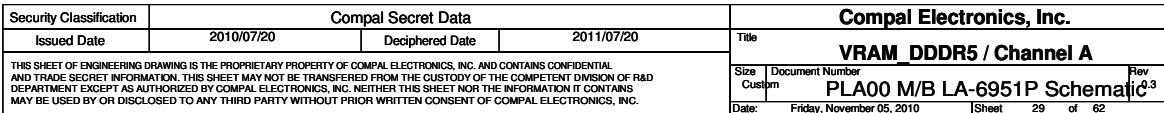
Mode G- Mapping

DATA Bus	
Address	0..31 32..63
CMD3	A4_BA2
CMD8	ABI#
CMD2	A2_BA0
CMD7	A6_A11
CMD15	RESET#
CMD13	RAS#
CMD4	A5_BA1
CMD6	A7_A8
CMD12	A0_A10
CMD10	CKE#
CMD9	A12_RFU
CMD1	A3_BA3
CMD11	A1_A9
CMD0	CS#
CMD5	WE#
CMD14	CAS#
CMD30	RAS#
CMD20	A3_BA3
CMD16	WE#
CMD25	A12_RFU
CMD28	A7_A8
CMD22	A0_A10
CMD19	A2_BA0
CMD17	A5_BA1
CMD27	A6_A11
CMD29	CAS#
CMD18	A4_BA2
CMD15	RESET#
CMD26	CKE#
CMD23	A1_A9
CMD24	ABI#
CMD21	CS#

MF=0
Byte 0 and 2



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SGRAM GDDR5

5GQ1H24AFR-T2L_BGA170

X76_HYN@

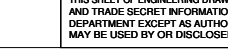
X76_HYN@



SGRAM GDDR5

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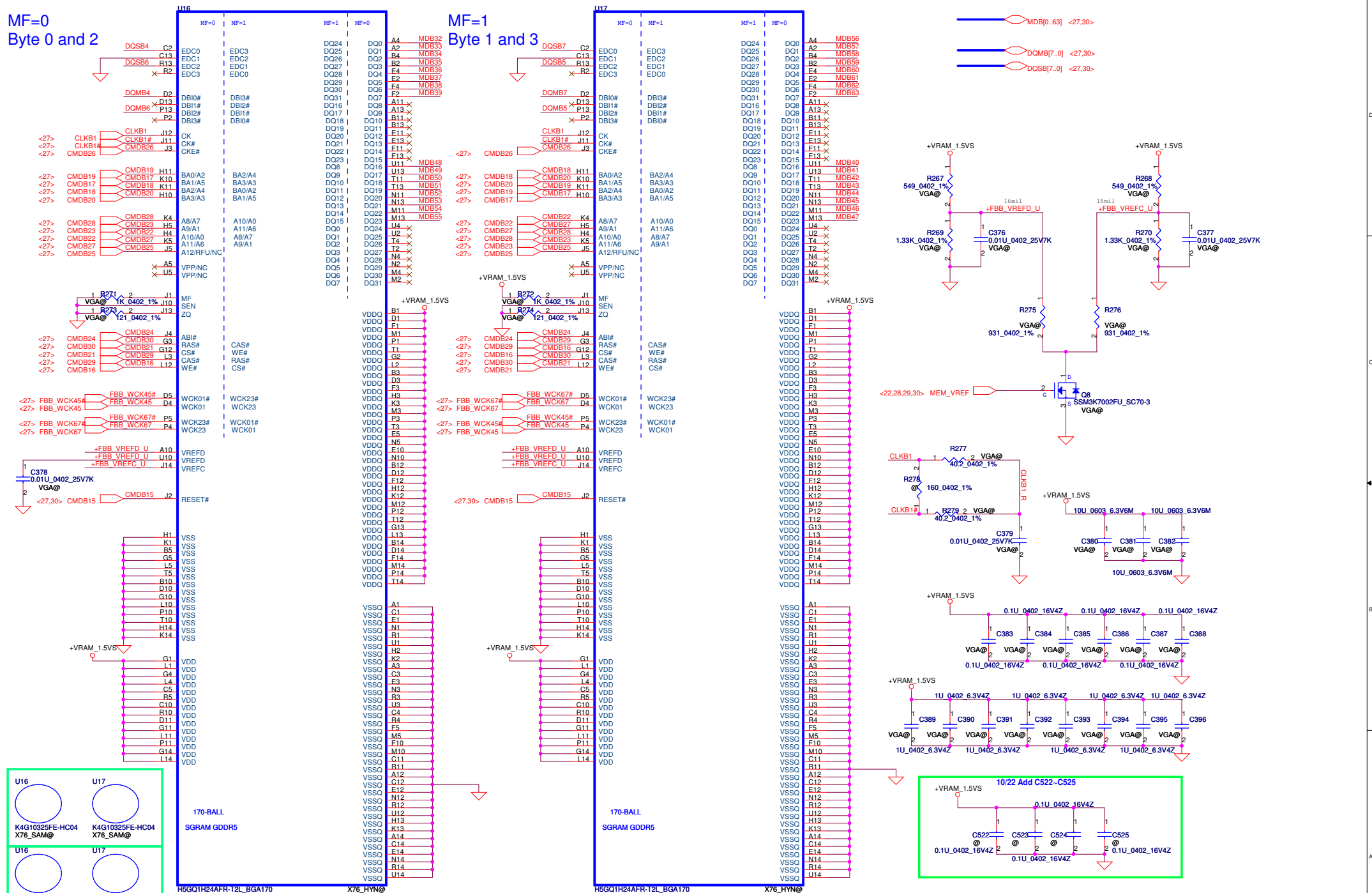
4AFR-T2L_BGA170



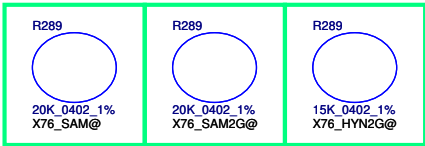
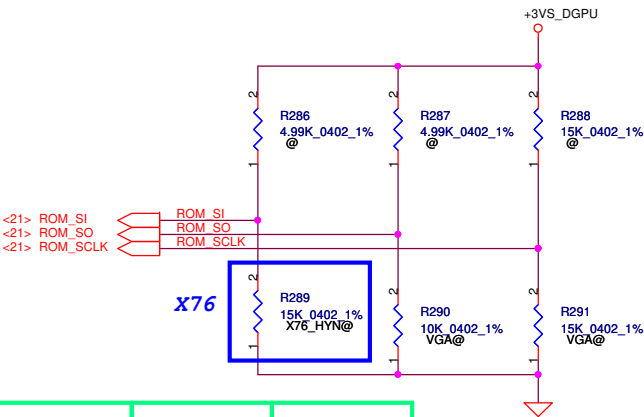
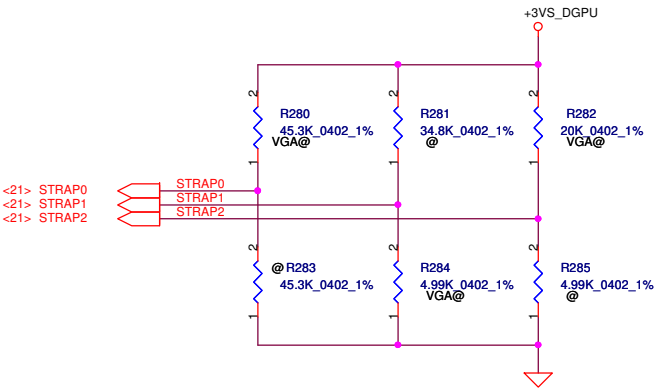
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	VRAM GDDR5 / Channel B	
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				Custom	PLA00 M/B LA-6951P Schematic	0.3
				Date:	Friday, November 05, 2010	Sheet

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3



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				Size	Document Number	Rev
				Custm	PLA00 M/B LA-6951P Schematic	0.3
Date:	Friday, November 05, 2010	Sheet	31	of 62		



Hynix H5GQ1H24AFR-T2L SA00003WL00	1G	0010	PD 15K
Samsung K4G10325FE-HC04 SA00003RS00	1G	0011	PD 20K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

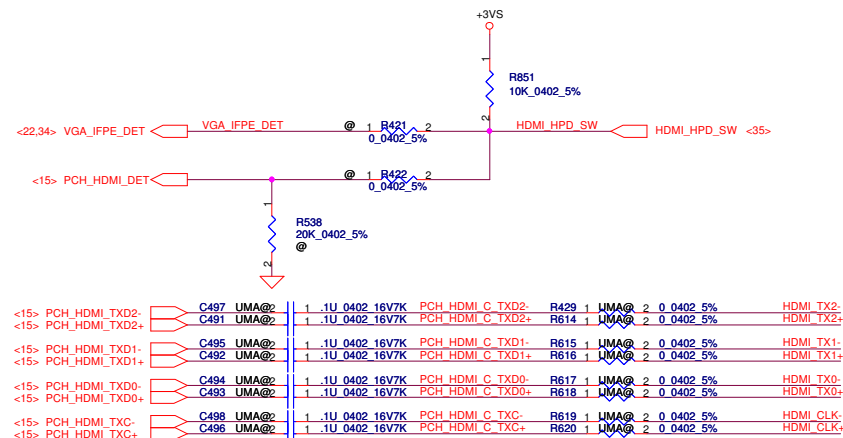
PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

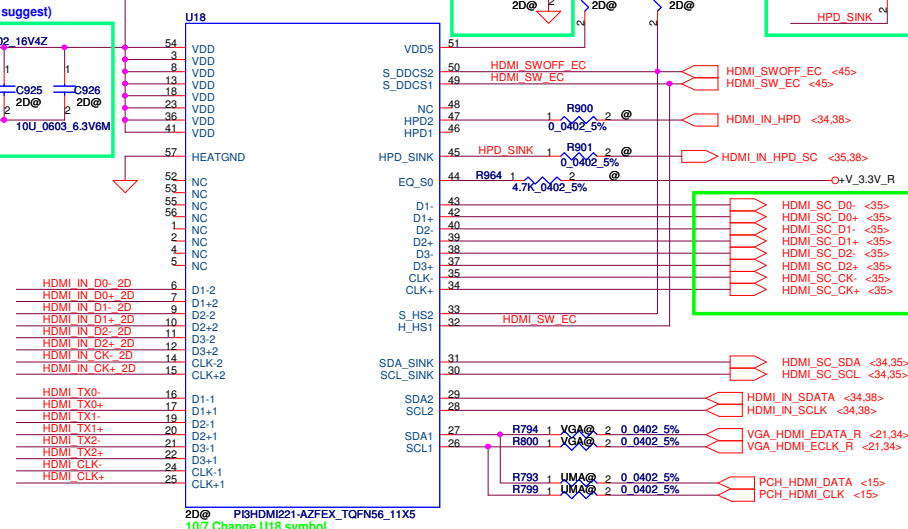
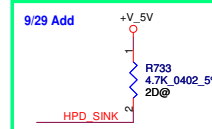
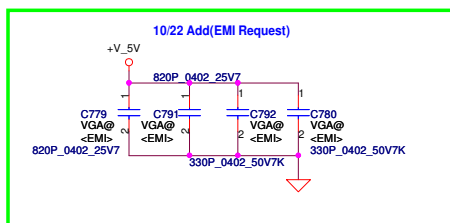
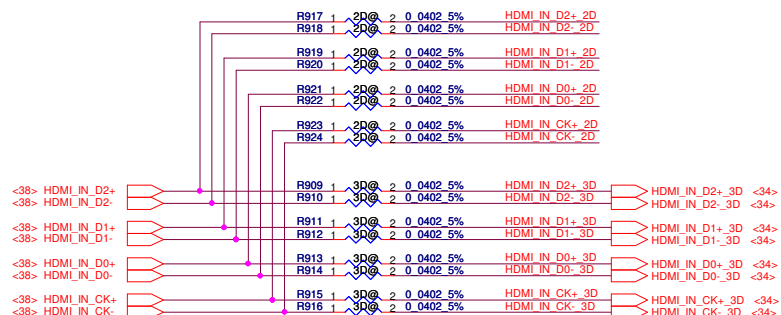
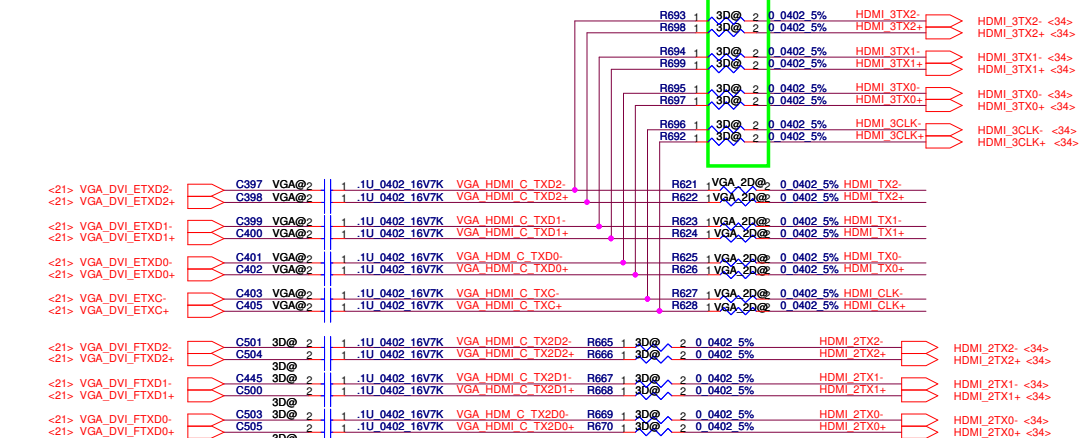
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

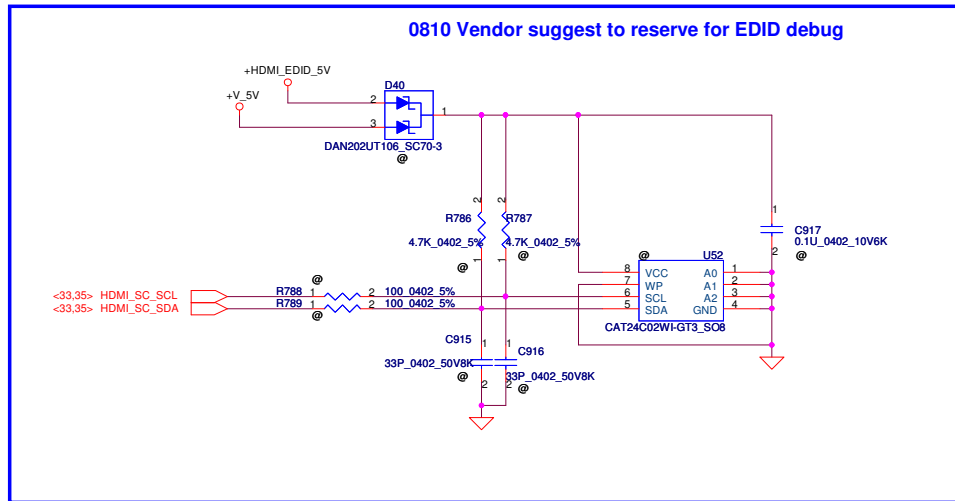
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	VGA(12/12)-MISC	
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				Date:	Friday, November 05, 2010	Sheet 32 of 62



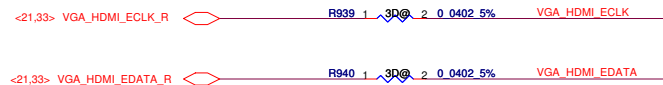
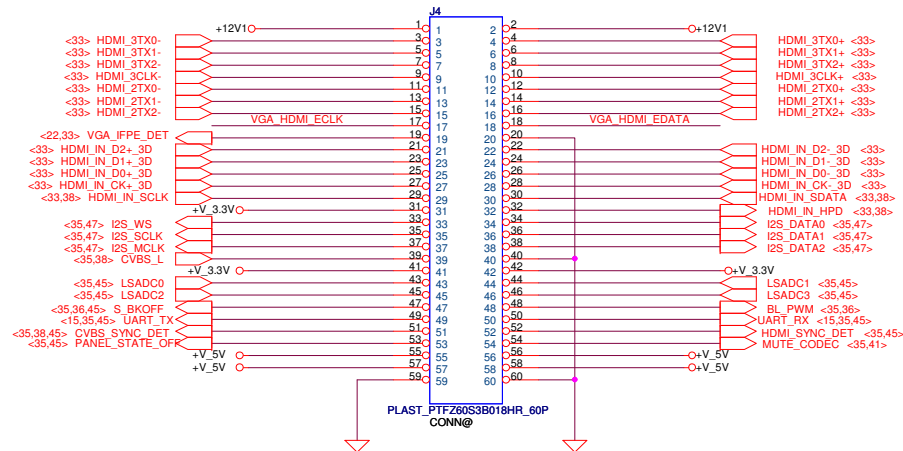
SEL2 (pin50)	SEL1 (pin49)	TMDS/I2C output
H	H	PORT1/SCL1/SDA1
H	L	PORT2/SCL2/SDA2



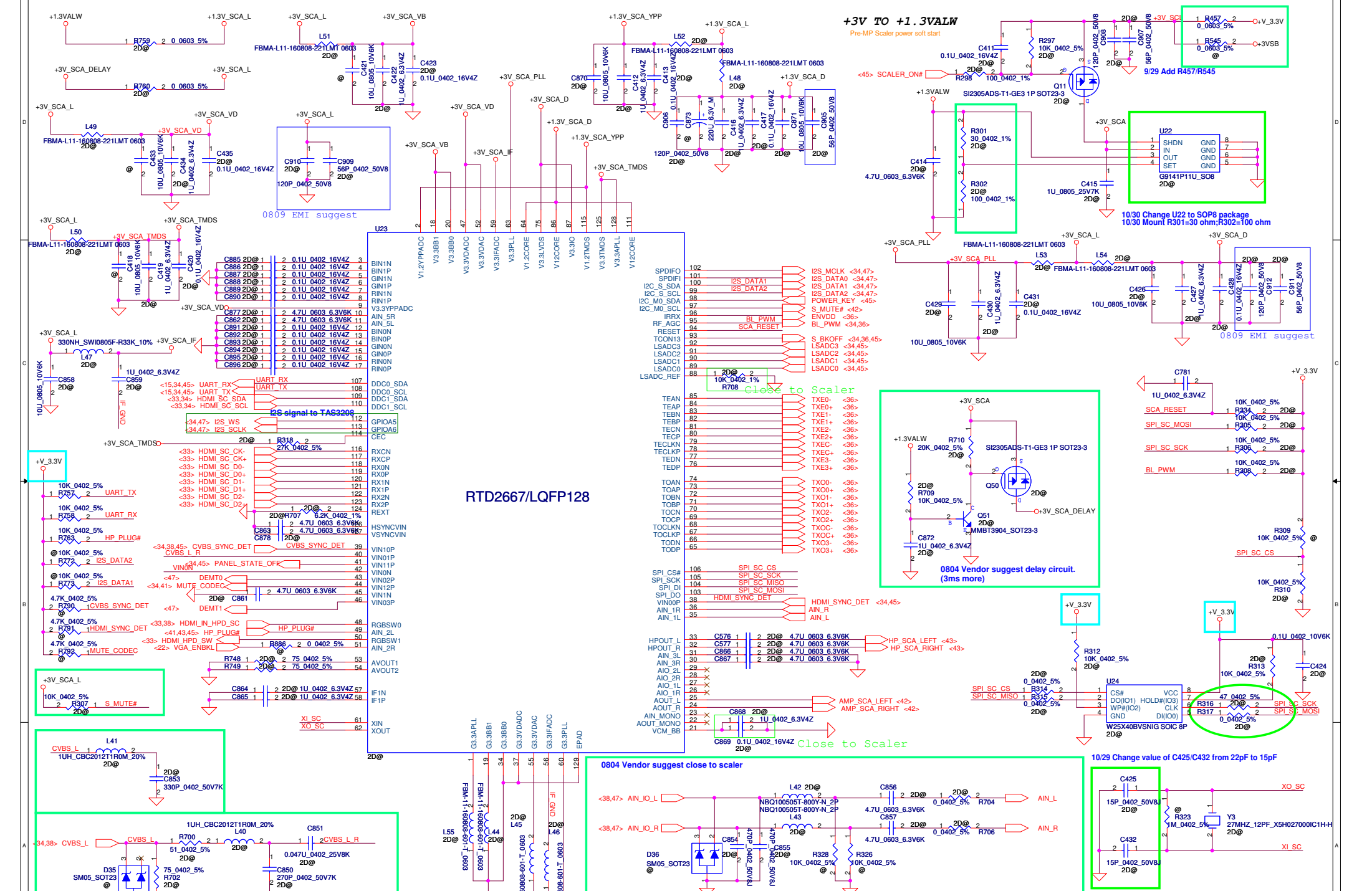
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	HDMI Switch	
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				Date:	Friday, November 05, 2010	Sheet



1003 IO/B Pin define update

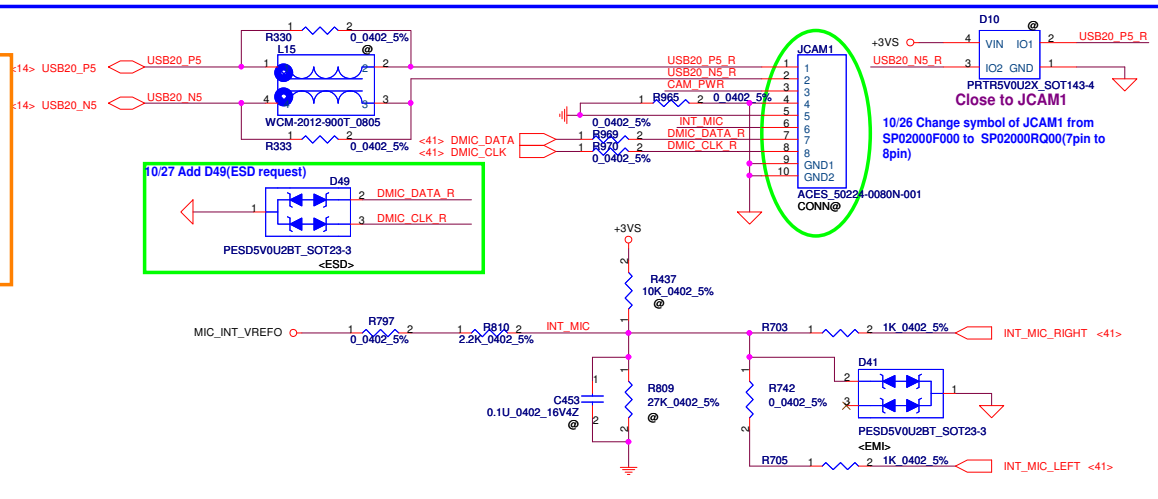


Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2010/07/20		Deciphered Date		2011/07/20		
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				3D Scalar				
				Size	Document Number			Rev
				Custom	PLA00 M/B LA-6951P Schematic			0.3
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Size	Document Number	PLA00 M/B LA-6951P Schematic				Rev 0.3		
Custom								
Date:	Friday, November 05, 2010	Sheet	35	of	62			

5/18 Change R332 from 100K to 10K ohm



JLVDS1

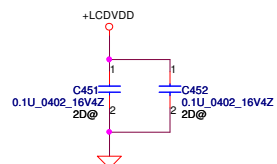
Pin	Signal	Pin	Signal
1	TX00+	1	TX00-
2	TX01+	2	TX01-
3	TX02+	3	TX02-
4	TX0C	4	TX0C+
5	TX03+	5	TX03-
6	TX04+	6	TX04-
7	TX05+	7	TX05-
8	TX06+	8	TX06-
9	TX07+	9	TX07-
10	TX08+	10	TX08-
11	TX09+	11	TX09-
12	TX00-	12	TX00+
13	TX01-	13	TX01+
14	TX02-	14	TX02+
15	TX0C+	15	TX0C-
16	TX03-	16	TX03+
17	TX04-	17	TX04+
18	TX05-	18	TX05+
19	TX06-	19	TX06+
20	TXE1-	20	TXE1+
21	TXE2-	21	TXE2+
22	TXE3-	22	TXE3+
23	TXE1+	23	TXE1-
24	TXE2+	24	TXE2-
25	TXE3+	25	TXE3-
26	LCDVDD	26	LCDVDD
27	GND	27	GND
28	GND	28	GND
29	GND	29	GND
30	GND	30	GND
31	GND	31	GND
32	GND	32	GND

ACES_87242-3001-09

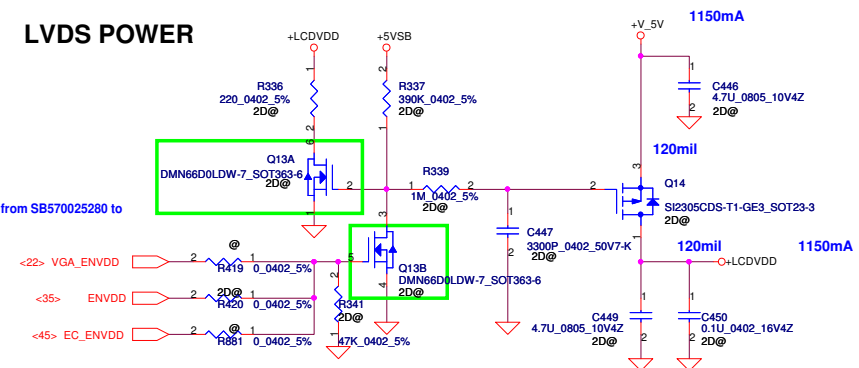
CONN@

C448
20@
680P_0402_50V7K

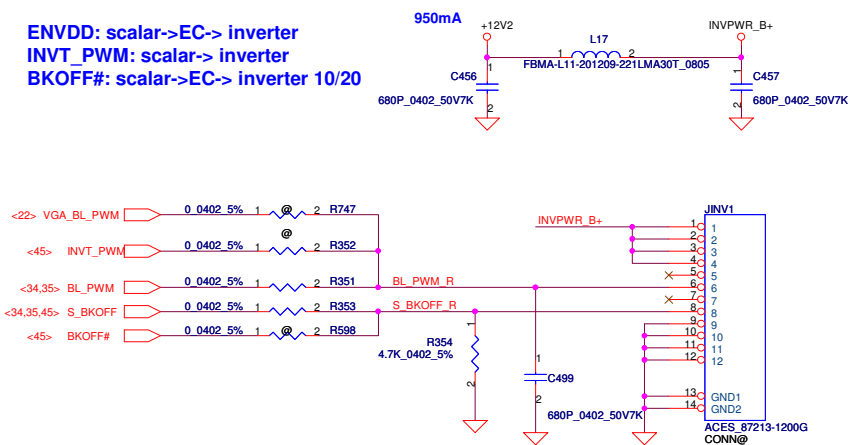
LCDVDD



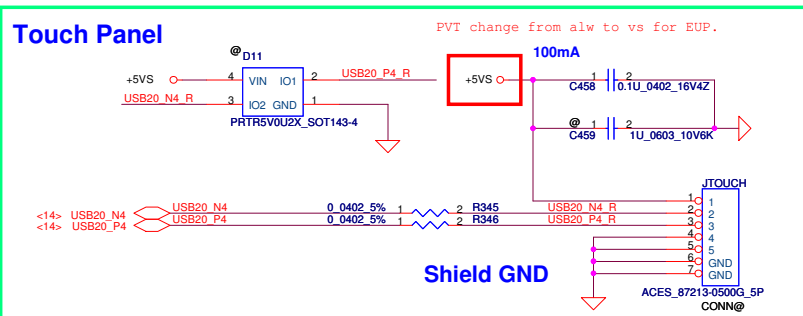
11/4 Change PN of Q13 from SB570025280 to SB000000DH00



ENVDD: scalar->EC-> inverter
INVT_PWM: scalar-> inverter
BKOFF#: scalar->EC-> inverter 10/20

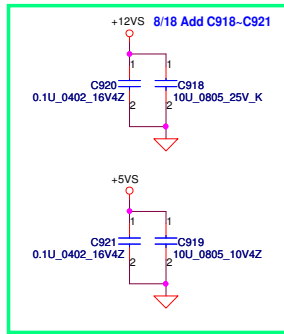


PVT change from alw to vs for EUP.



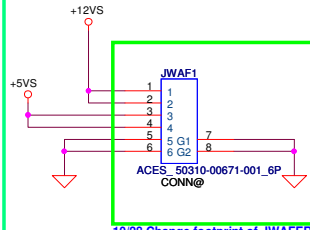
Security Classification		Compal Secret Data		Compal Electronics, Inc. Title LCD CONN. / WebCam	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Size	Document Number PLA00 M/B LA-6951P Schematic ³
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				Date:	Friday, November 05, 2010 Sheet 36 of 62

HDD POWER Conn



Layout Note: Place C918/C919/C920/C921 close to JWAFF1

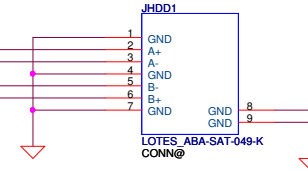
HDD



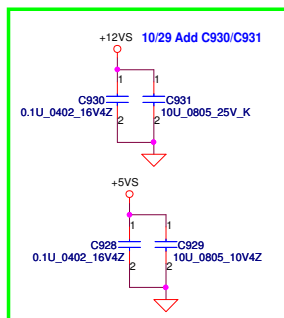
10/28 Change footprint of JWAFF1 from LTCX002XR00 to LTCX0033X00



SATA HDD Conn.

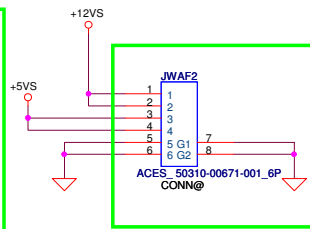


ODD POWER Conn



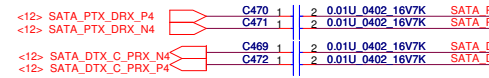
10/28 Add C928/C929

Layout Note: Place C928/C929 close to JWAFF2

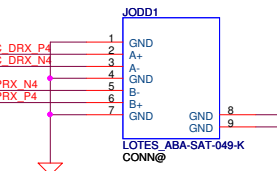


10/28 Add footprint of JWAFF2 to LTCX0033X00

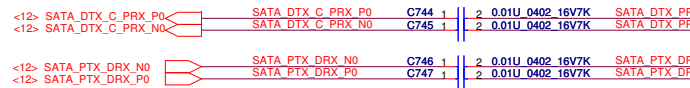
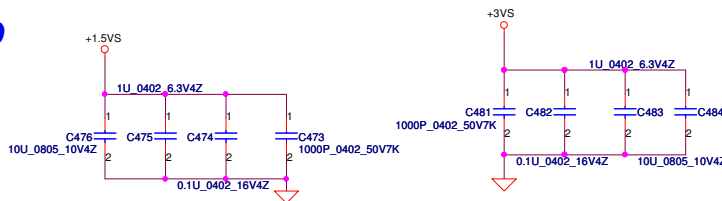
ODD



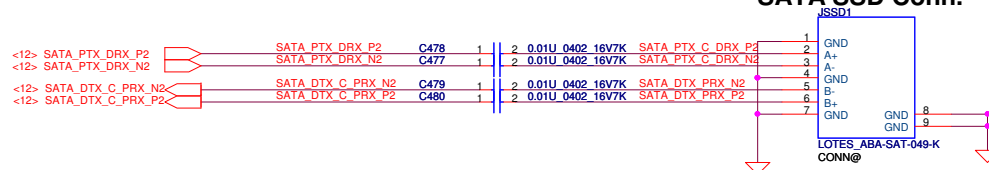
SATA ODD Conn.



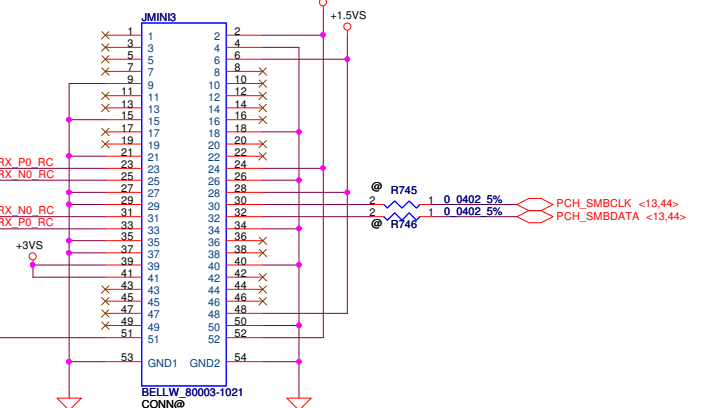
SSD



SATA SSD Conn.

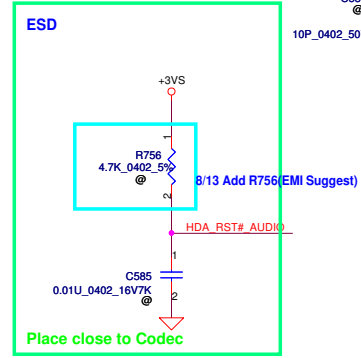
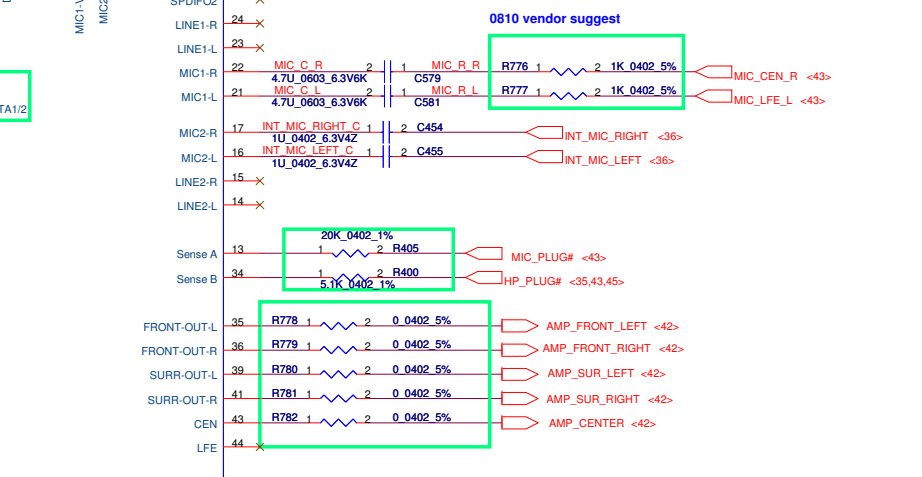
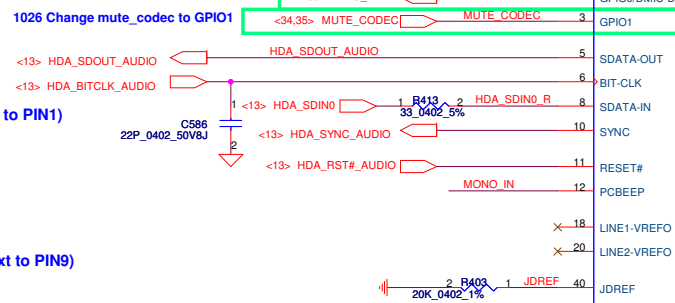
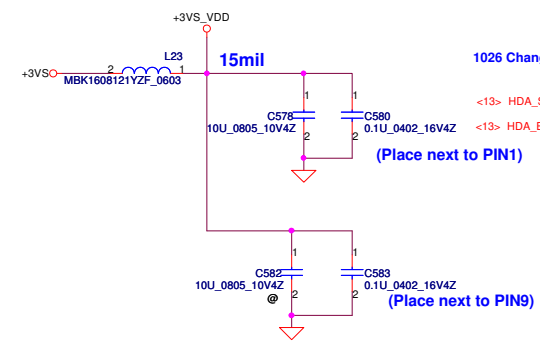
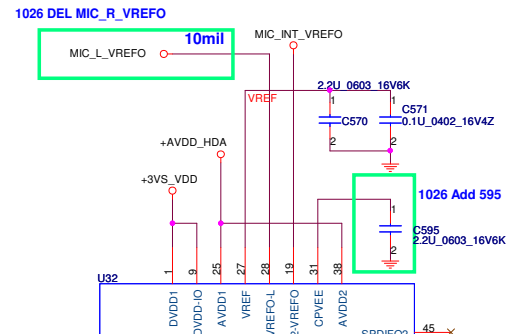
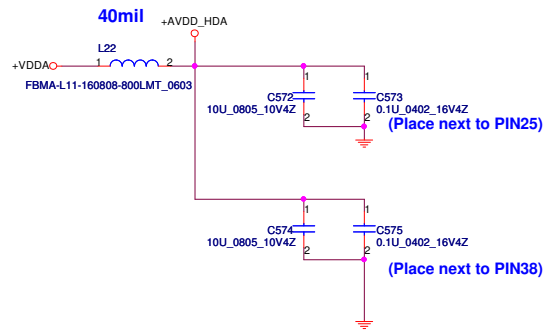
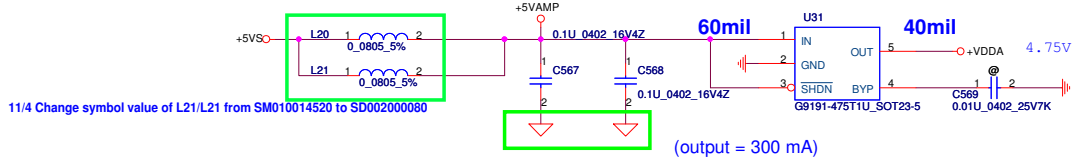
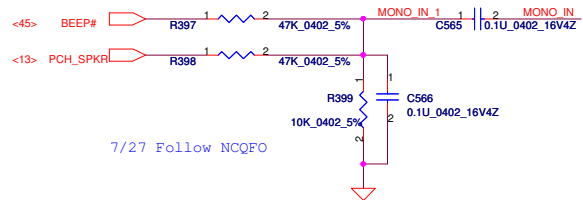


MINI SSD Conn.



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Size B		Document Number		PLA00 M/B LA-6951P Schematic	
Date: Friday, November 05, 2010		Sheet 37 of 62		Rev 0.3	





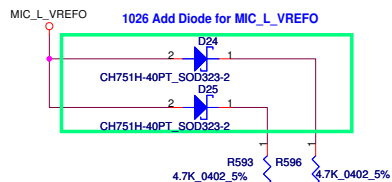
Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/07/20				Title			
Deciphered Date				2011/07/20				HD Audio Codec ALC663			
Size				Document Number				PLA00 M/B LA-6951P Schematic			
Date				Friday, November 05, 2010				Sheet 41 of 62			

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Issued Date		Deciphered Date		Size Custom	
2010/07/20		2011/07/20		Document Number PLA00 M/B LA-6951P Schematic	
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EXT MIC IN

4.7K_0402_5%

4.7K_0402_5%

4.7K_0402_5%

4.7K_0402_5%

4.7K_0402_5%

4.7K_0402_5%

4.7K_0402_5%

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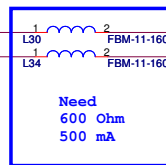
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4.7K_0402_5%

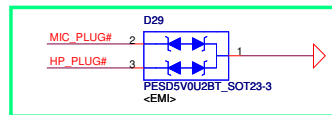
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4.7K_0402_5%

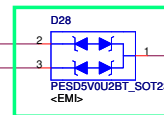
4.7K_0402_5%



8/13 Change symbol of D29 to SCA00000T00(EMI Suggest)

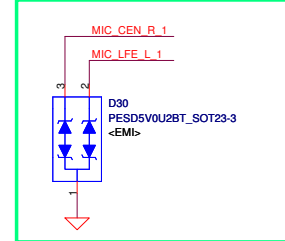


Add for EMC suggest

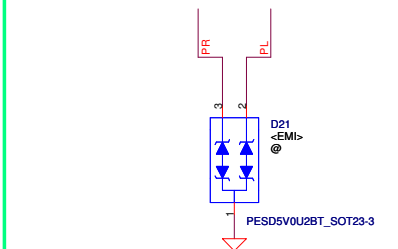


8/13 Change symbol of D28 to SCA00000T00(EMI Suggest)

8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)



8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)



HP OUT

<35> HP_SCA_RIGHT

<35> HP_SCA_LEFT

<41> HP_RIGHT

<41> HP_LEFT

<41> HP_RIGHT

<41> HP_LEFT

<41> HP_RIGHT

<41> HP_LEFT

<41> HP_RIGHT

<41> HP_LEFT

<41> HP_RIGHT

<41> HP_LEFT

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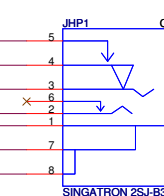
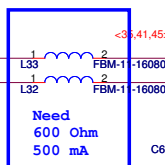
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<41> HP_LEFT

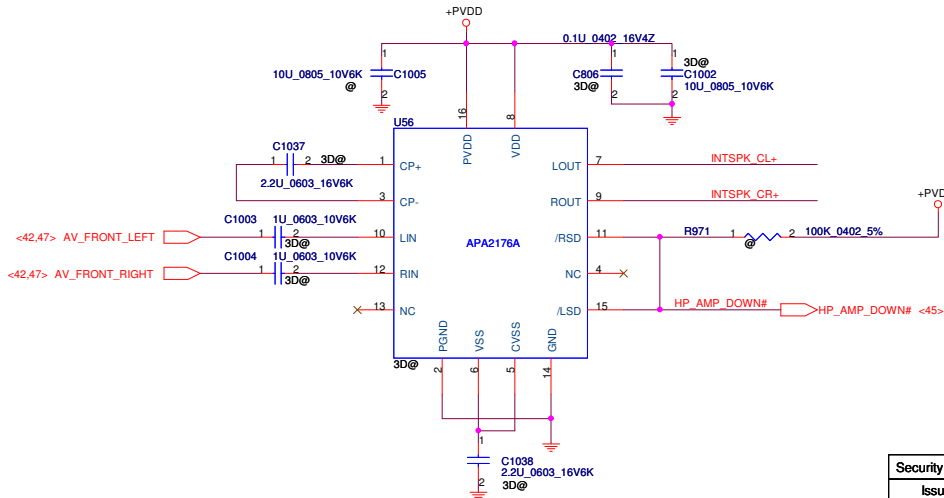
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<41> HP_LEFT

<41> HP_RIGHT

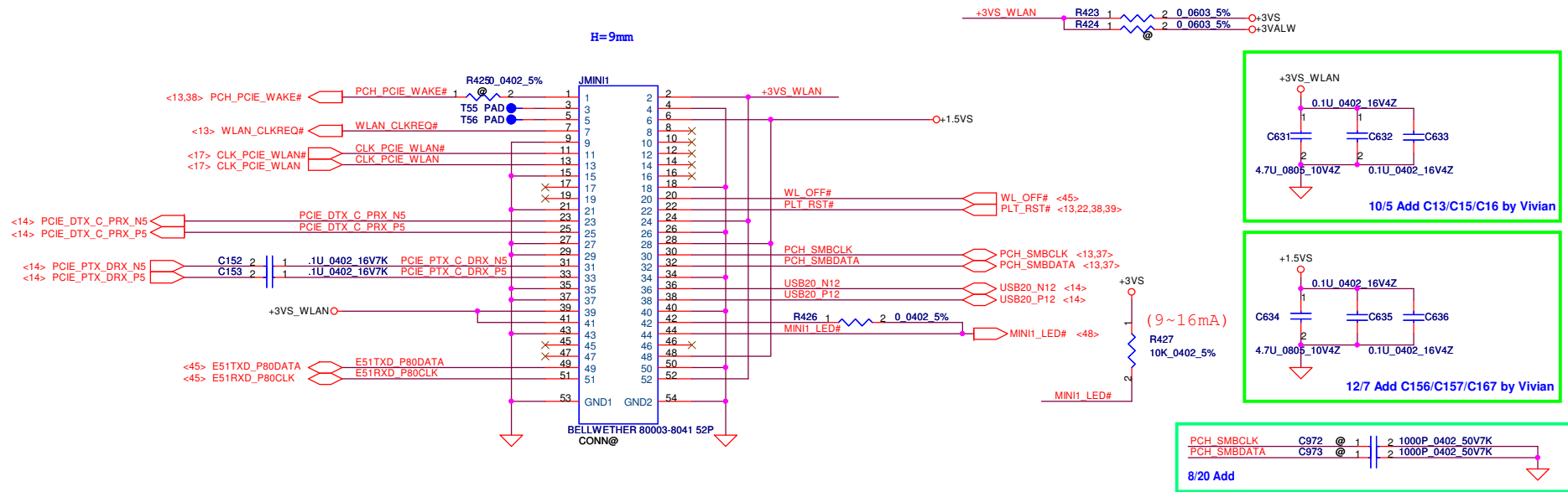


10/22 Change U56 from SA00001ZW00 to SA00004IS00



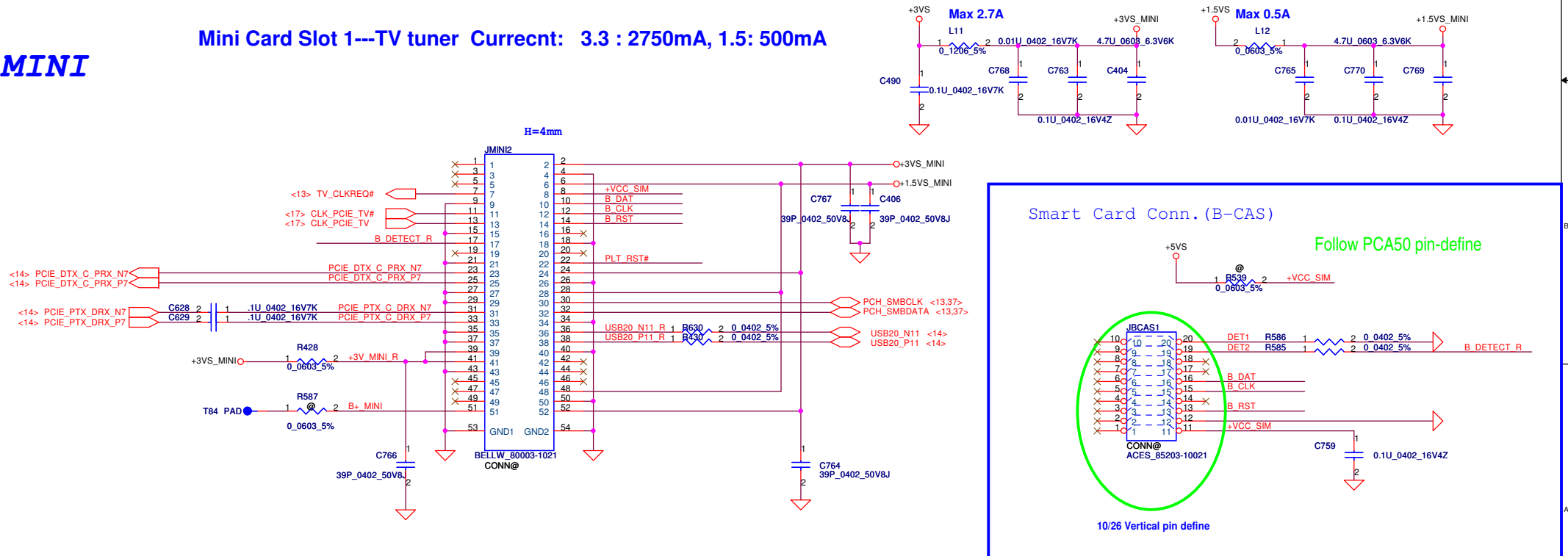
Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2010/07/20	Audio Jack
Deciphered Date	2011/07/20	PLA00 M/B LA-6951P Schematic
Size	Document Number	Rev 0.3
Customer	PLA00 M/B LA-6951P Schematic	
Date:	Friday, November 05, 2010	Sheet 43 of 62

WLAN



MINI

Mini Card Slot 1---TV tuner Currecnt: 3.3 : 2750mA, 1.5: 500mA

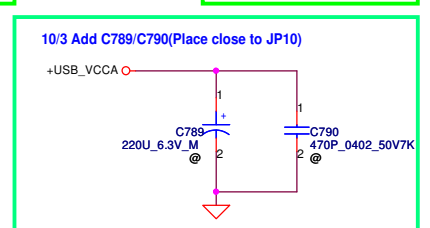
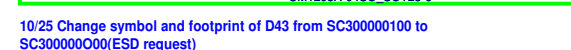
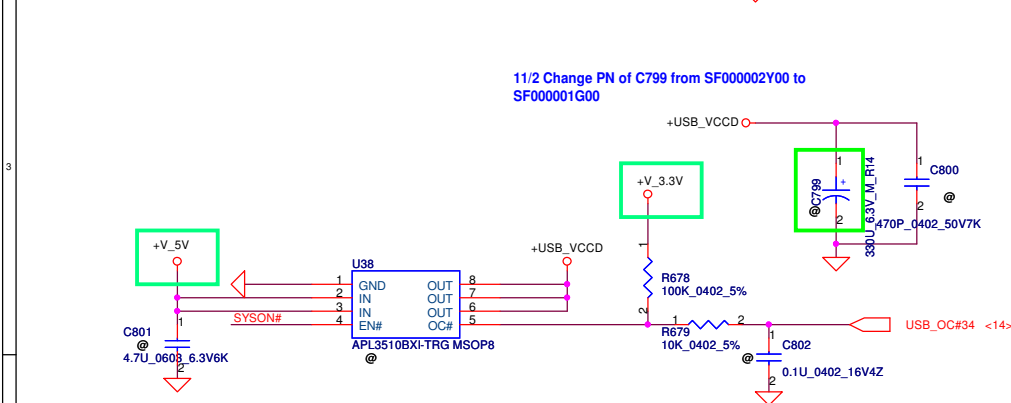
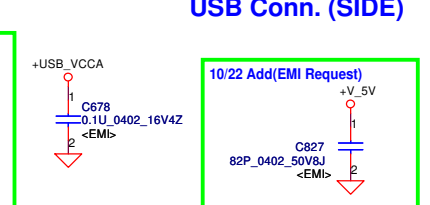
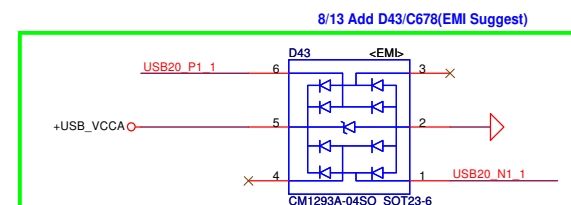
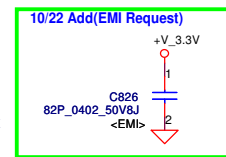
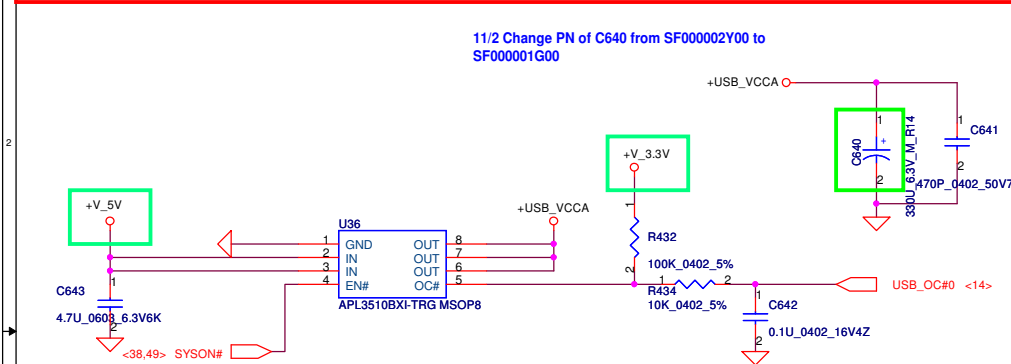
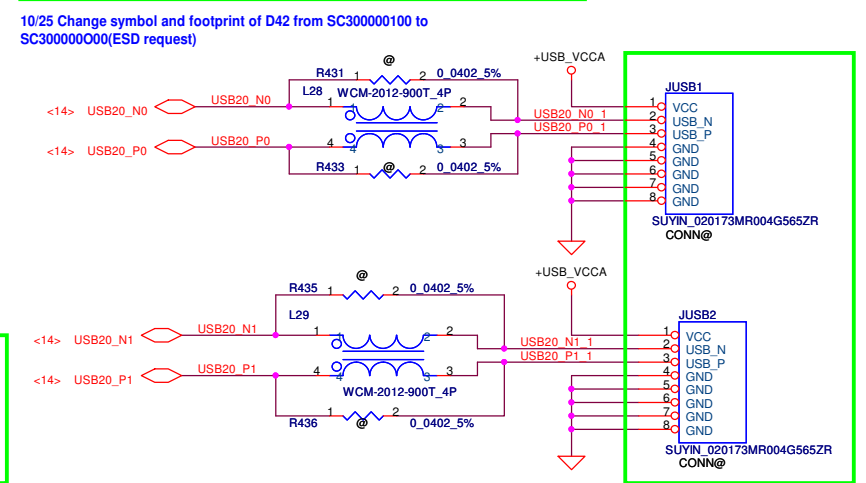
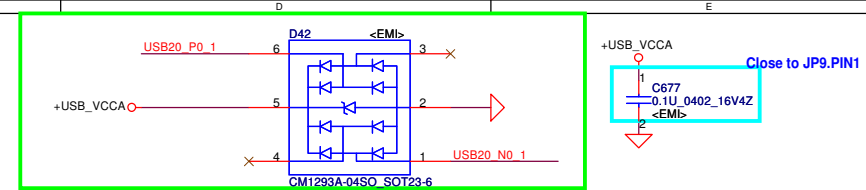
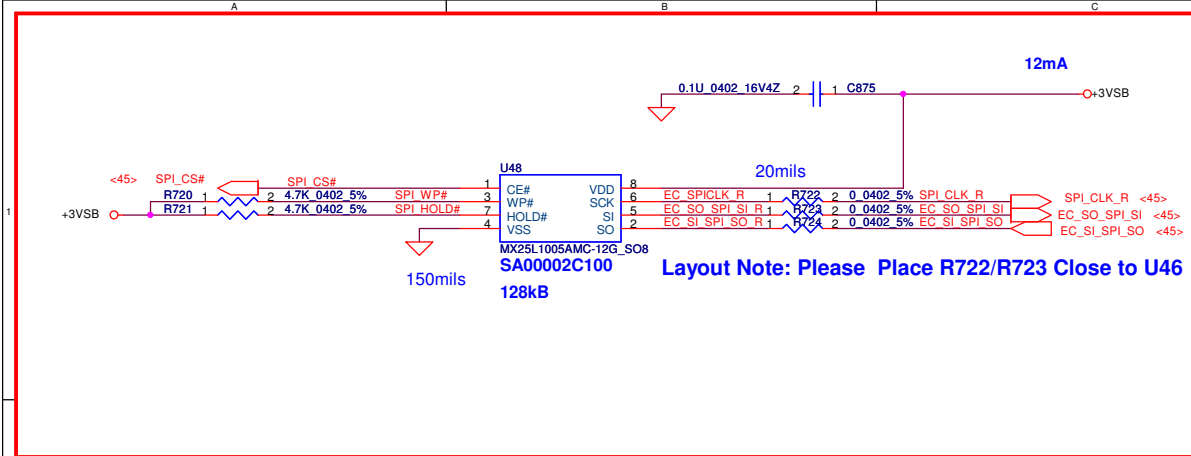


PCH SMBCLK C974 @ 1 2 1000P 0402 50V7K
PCH SMBDATA C975 @ 1 2 1000P 0402 50V7K
8/20 Add

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Size	Document Number	PLA00 M/B LA-6951P Schematic		Rev 0.3	
Date:	Friday, November 05, 2010	Sheet	44	of 62	

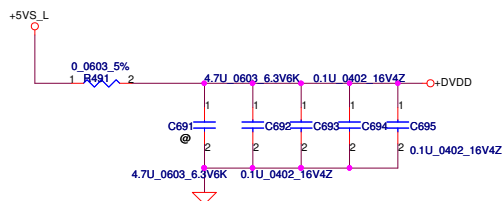
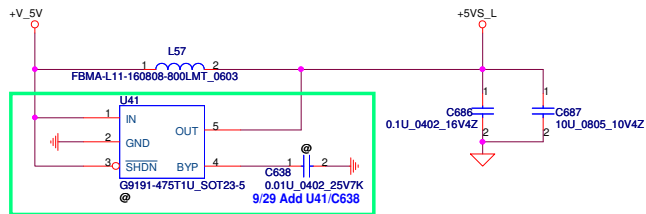


Security Classification		Compal Secret Data		Compal Electronics, Inc. EC KB930/KB conn	
Issued Date		2010/07/20		Title	
		Deciphered Date		2011/07/20	
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				Date: Friday, November 05, 2010 Sheet 45 of 62	

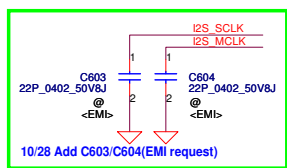
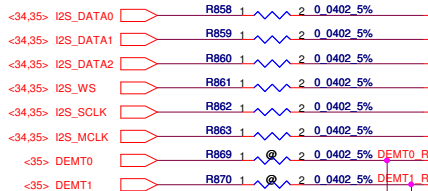
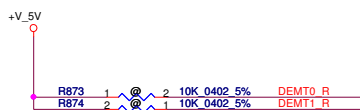
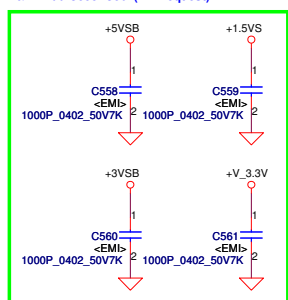


USB Conn. (SIDE)

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Size	Document Number	Rev		PLA00 M/B LA-6951P Schematic	
Date:	Friday, November 05, 2010	Sheet	46 of 62		

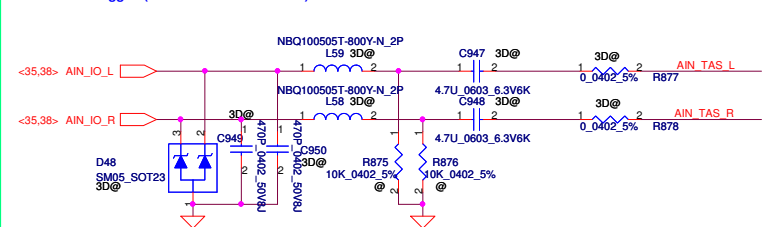


10/27 Add C558-C561(EMI request)



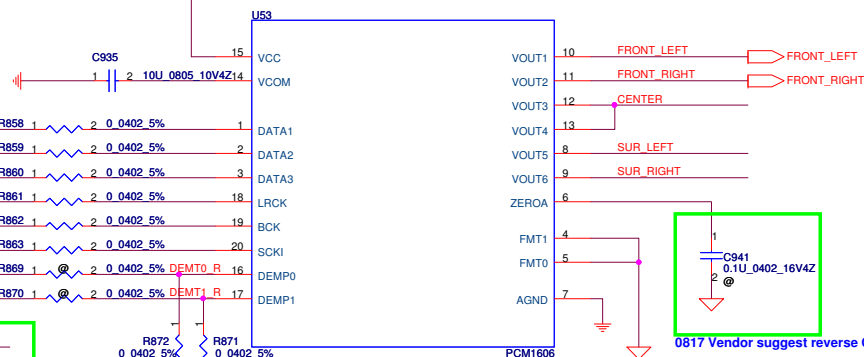
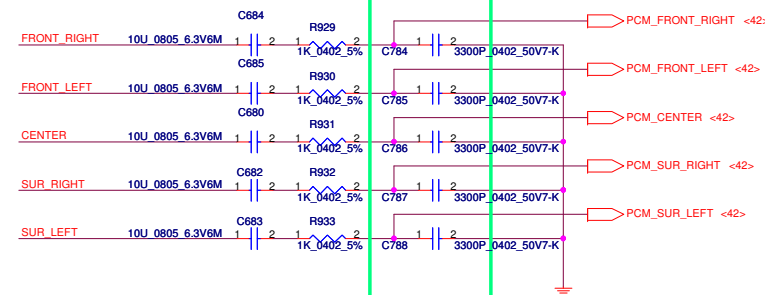
10/28 Add C603/C604(EMI request)

0818 Vendor suggest(Close to U42.Pin43/Pin44)



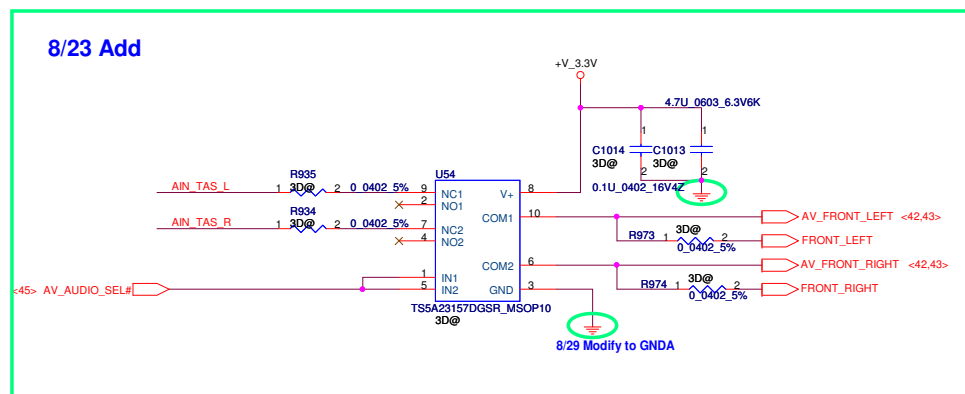
De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

10/3 Change symbol location



0817 Vendor suggest reverse C to GND

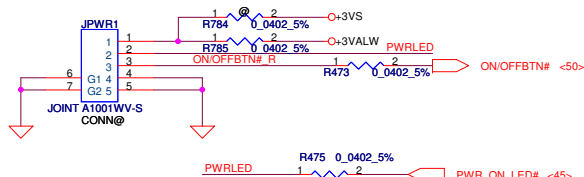
8/23 Add



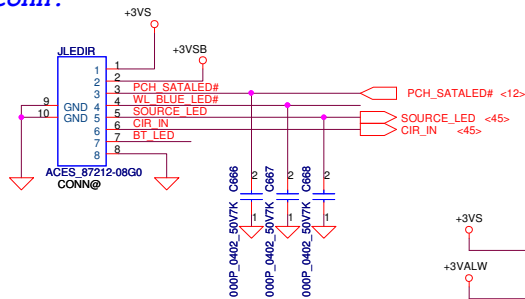
8/29 Modify to GND

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				Date:	Friday, November 05, 2010
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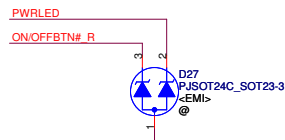
Power switch board



LED board conn.

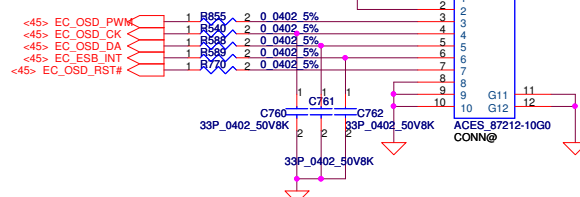


8/13 Change symbol of D27 to SCA0000E00(EMI Suggest)

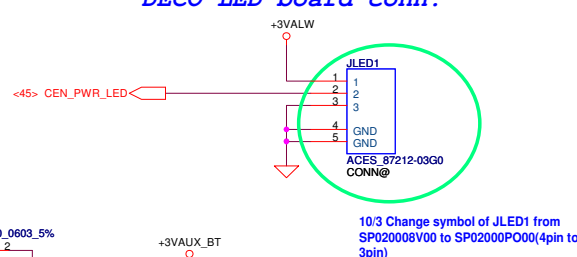


SENSOR BOTTOM

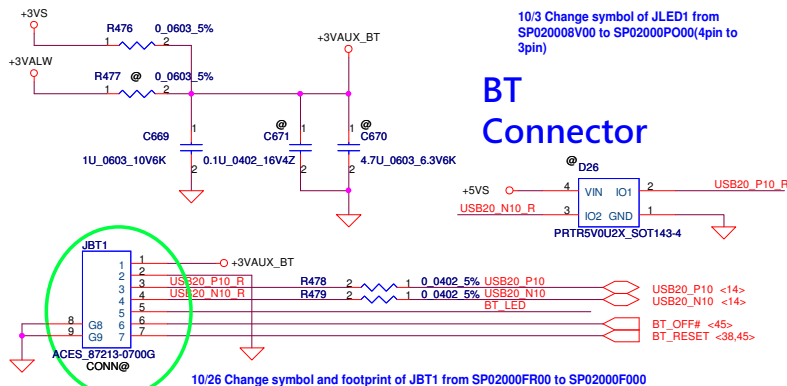
Follow NCQD0



DECO LED board conn.

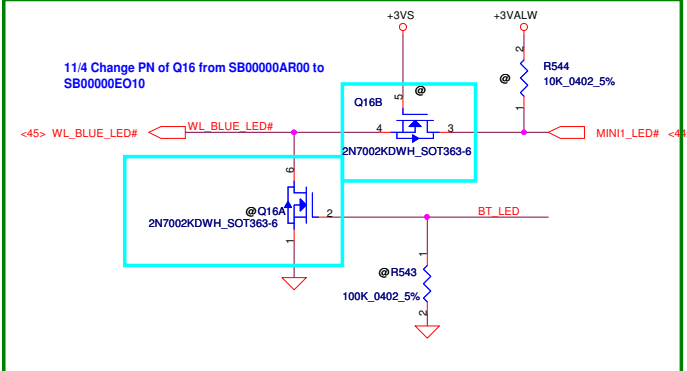


BT Connector

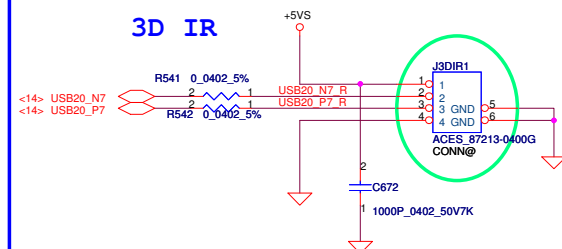


10/26 Change symbol and footprint of JBT1 from SP02000FR00 to SP02000F000

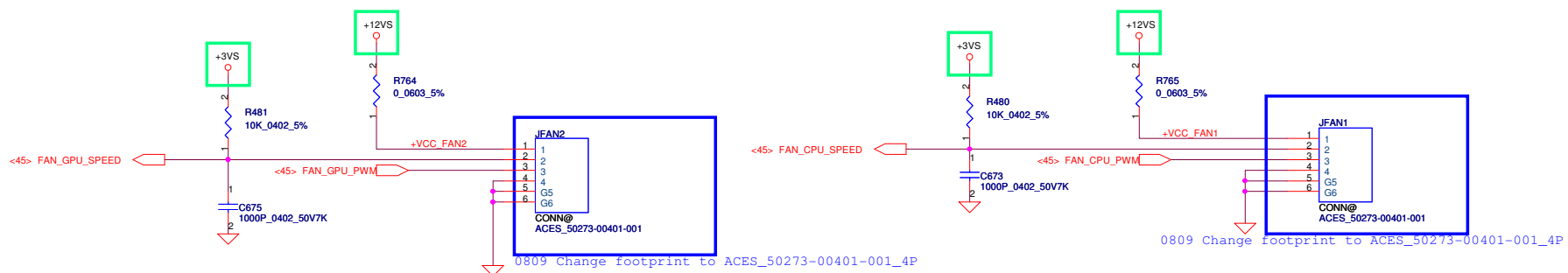
11/4 Change PN of Q16 from SB00000AR00 to SB00000EO10



3D IR

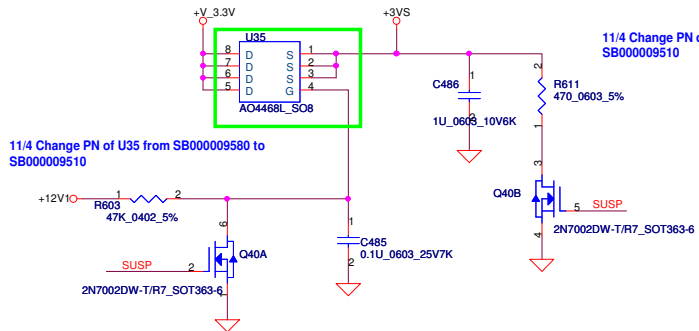


Fan Control circuit

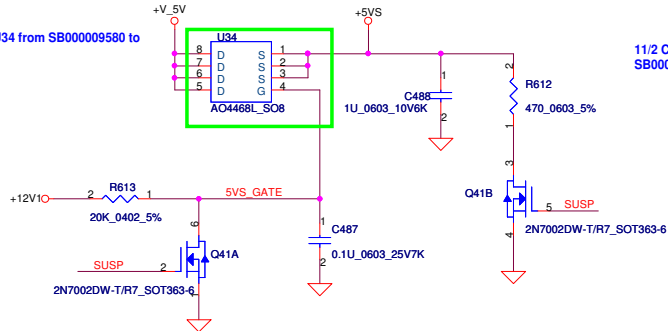


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Size	Document Number	PLA00 M/B LA-6951P Schematic		Rev	0.3
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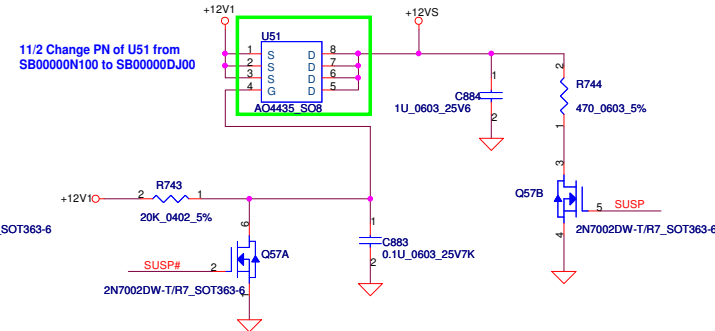
+V_3.3V TO +3VS



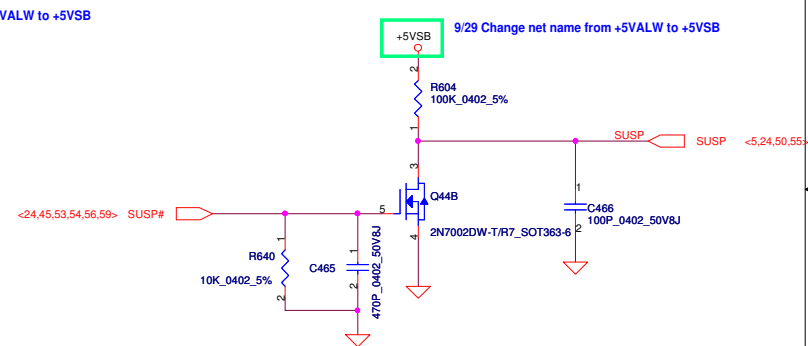
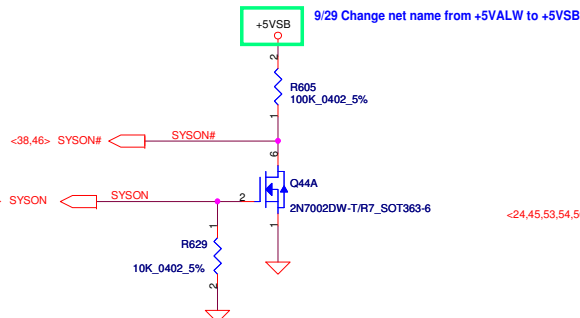
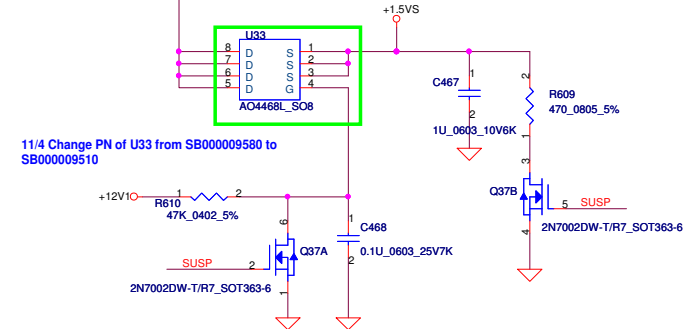
+V_5V TO +5VS



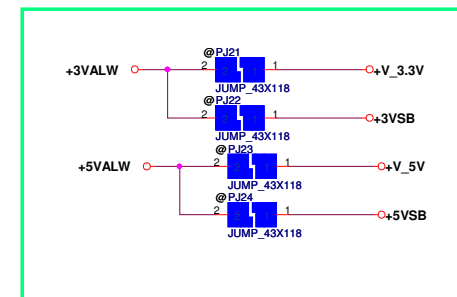
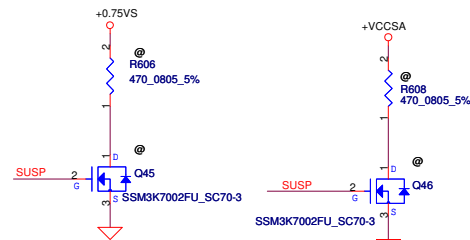
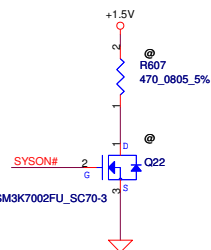
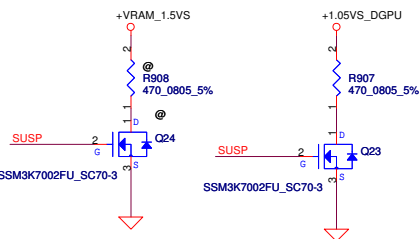
+12V1 TO +12VS



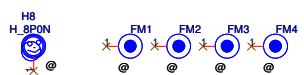
+1.5V TO +1.5VS



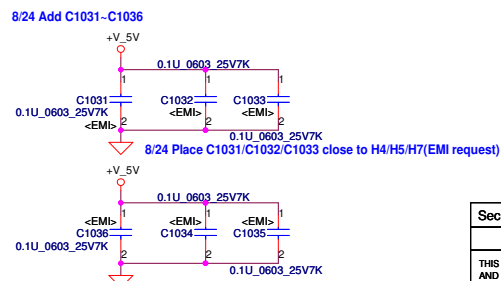
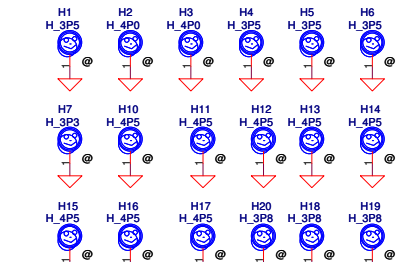
Discharge circuit



NON-PDH

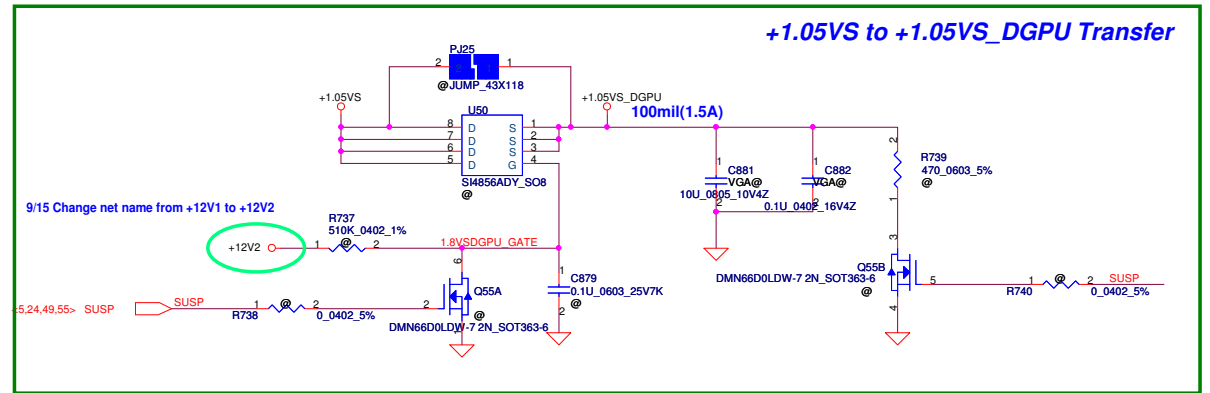
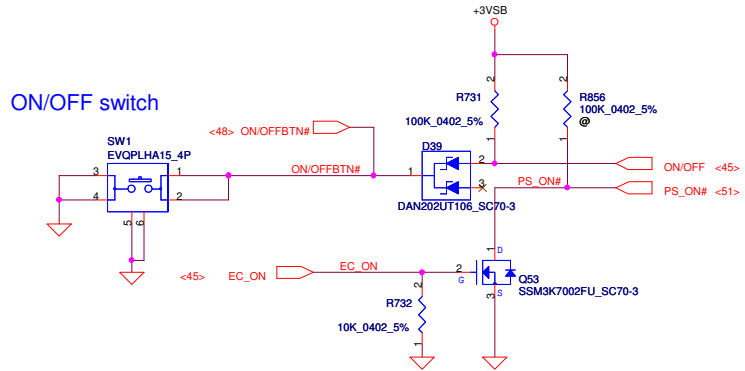


Screw



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				PLA00 M/B LA-6951P Schematic	
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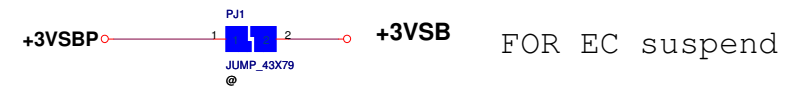
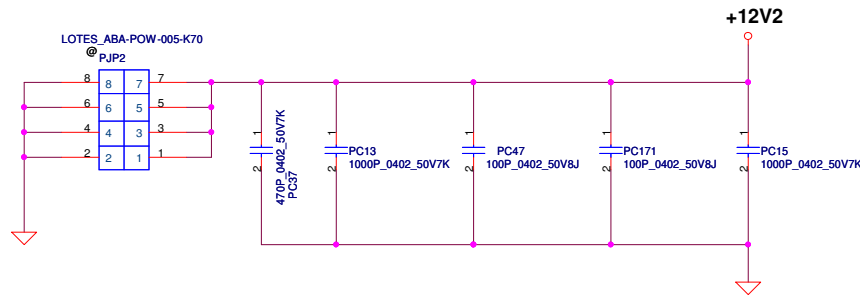
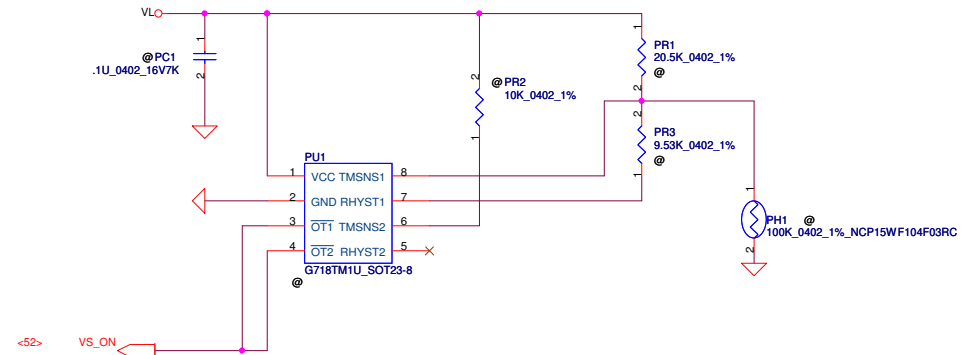
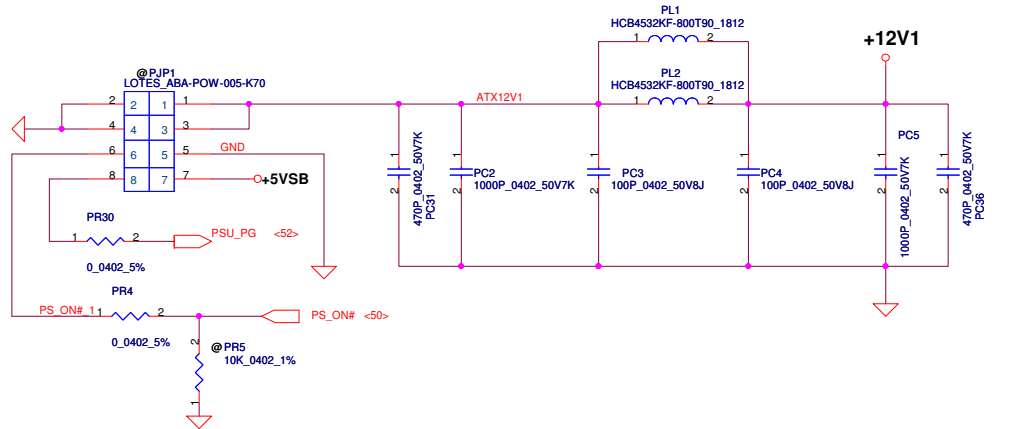
Power Button



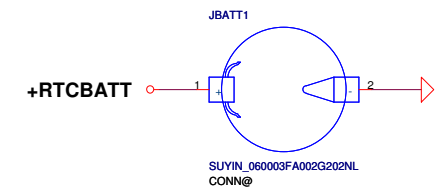
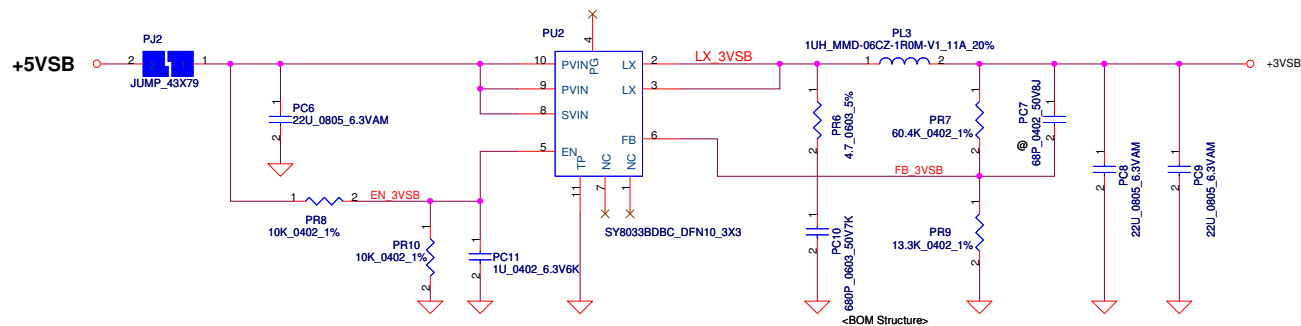
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	Power OK/PBN
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PH1 under CPU botten side :

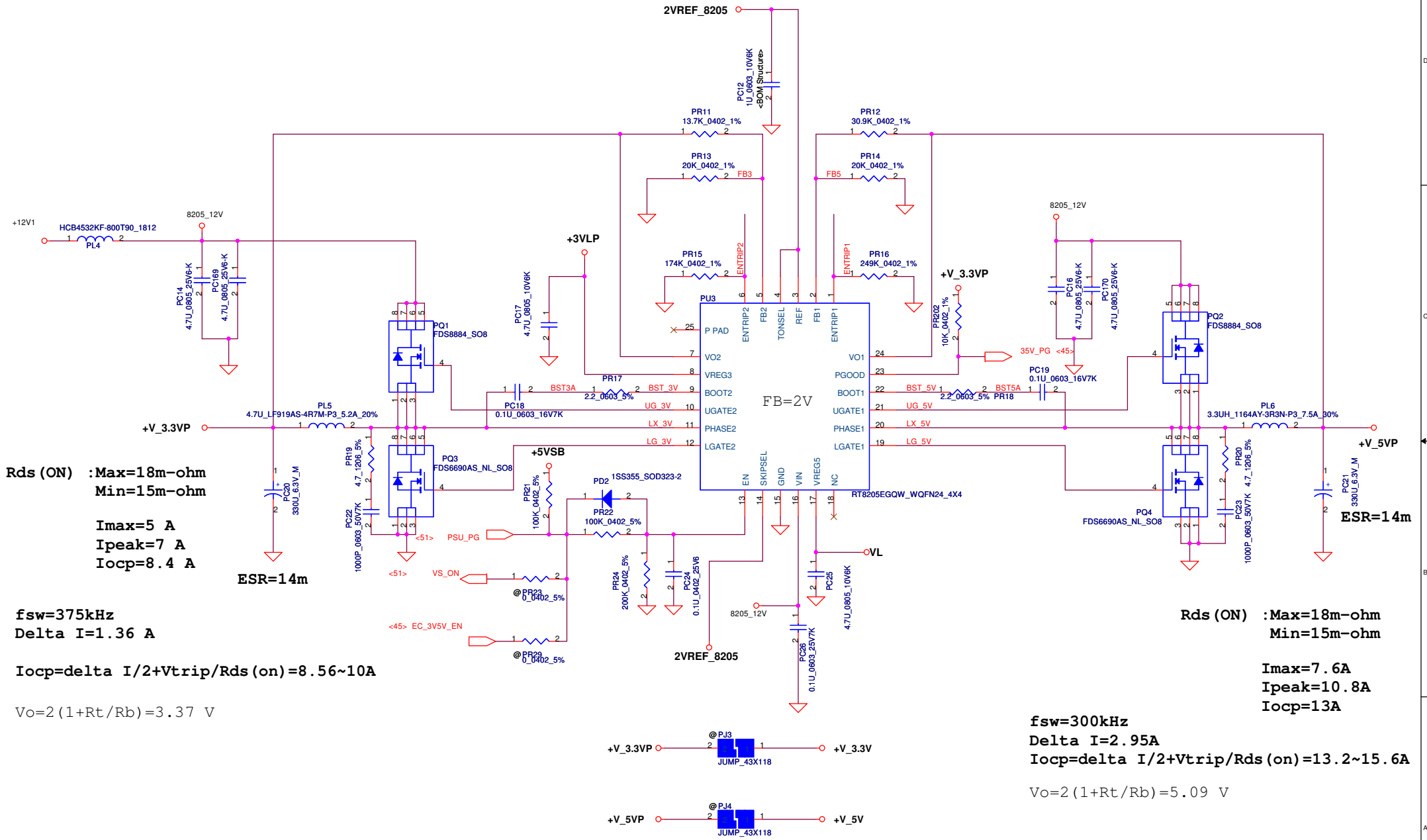
CPU thermal protection at 92 degree C
Recovery at 57 degree C



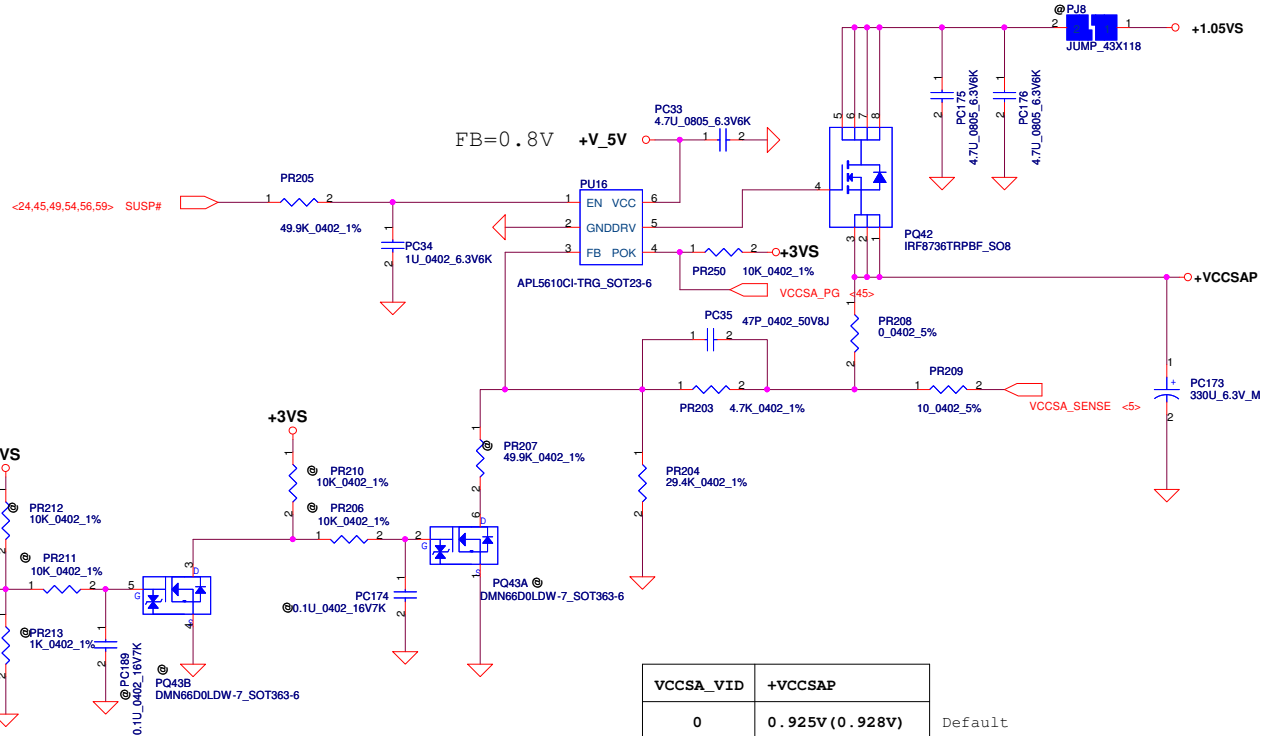
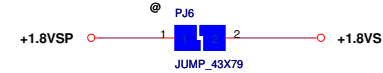
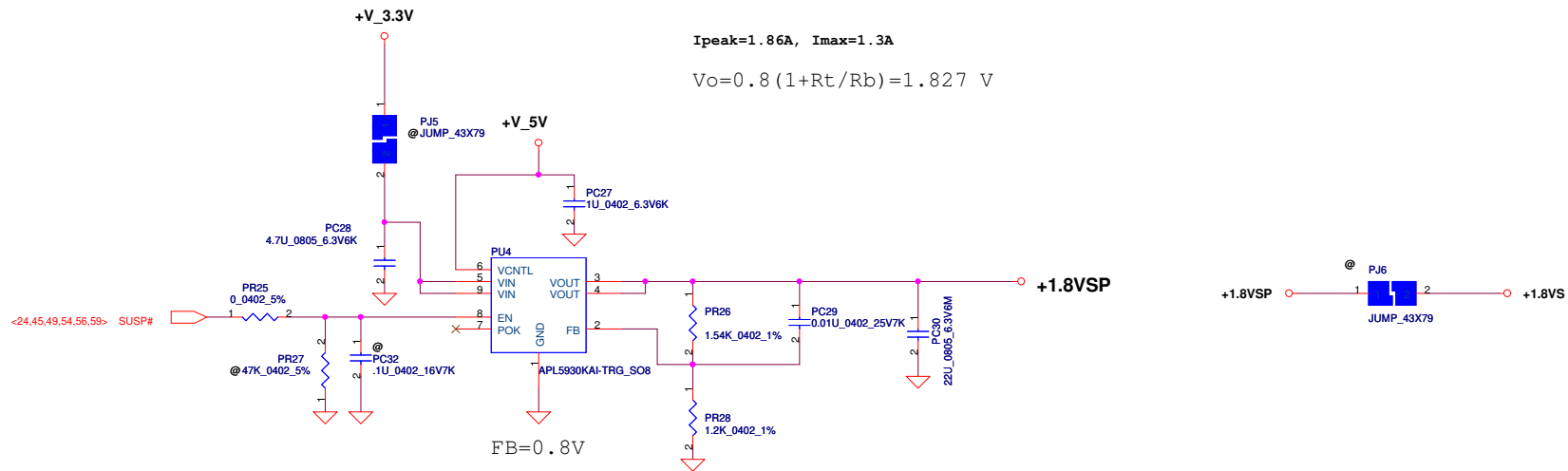
$V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR7/PR9) = 3.318 V$
 $I_{peak} = 0.062A, I_{max} = 0.045A$
Current limit >4A



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								Custom			Document Number	
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Size	Document Number	0.3		Rev	
Date:	Friday, November 05, 2010	Sheet	52 of 62		

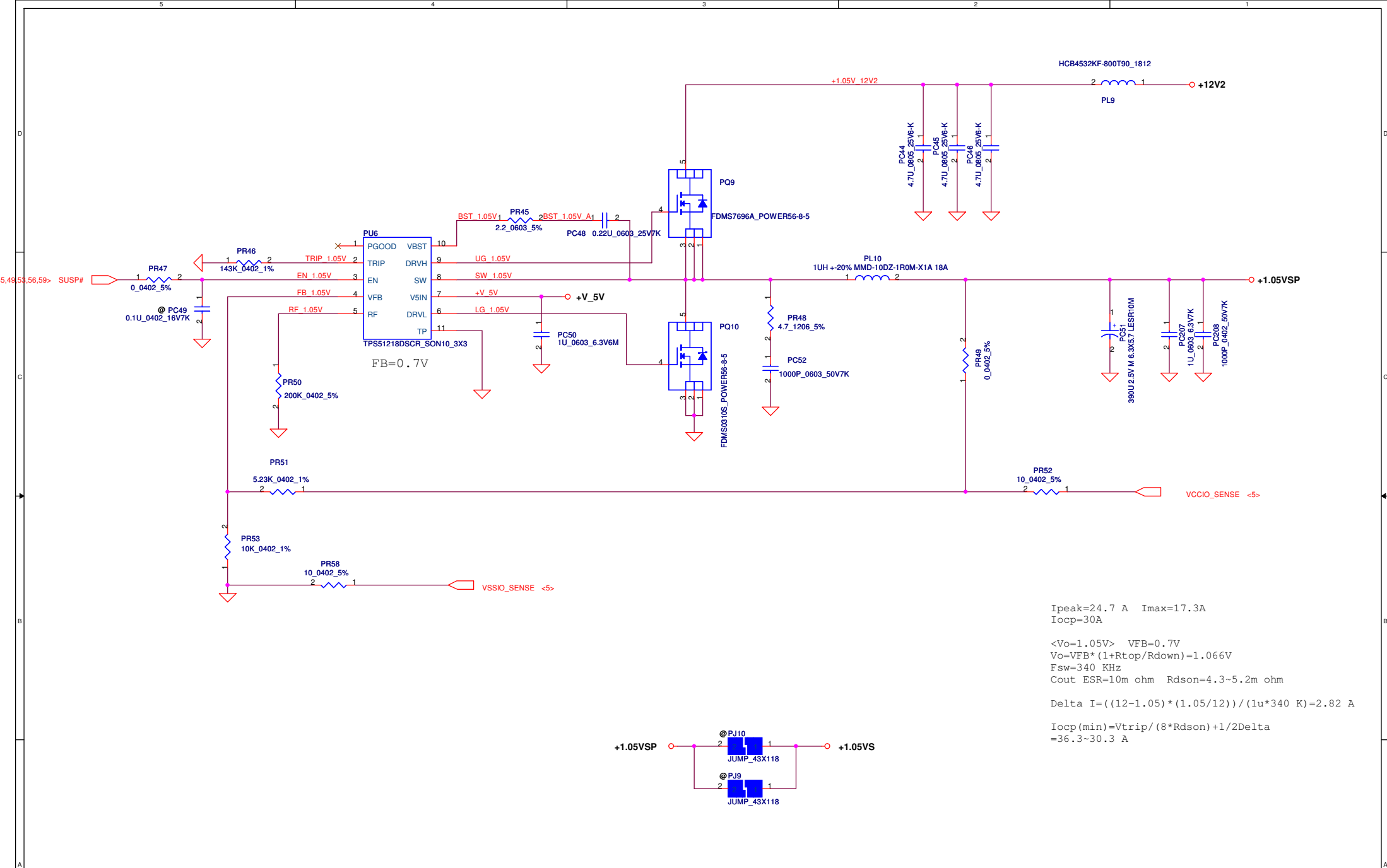


VCCSA_VID	+VCCSAP
0	0.925V (0.928V)
1	0.85V (0.851V)

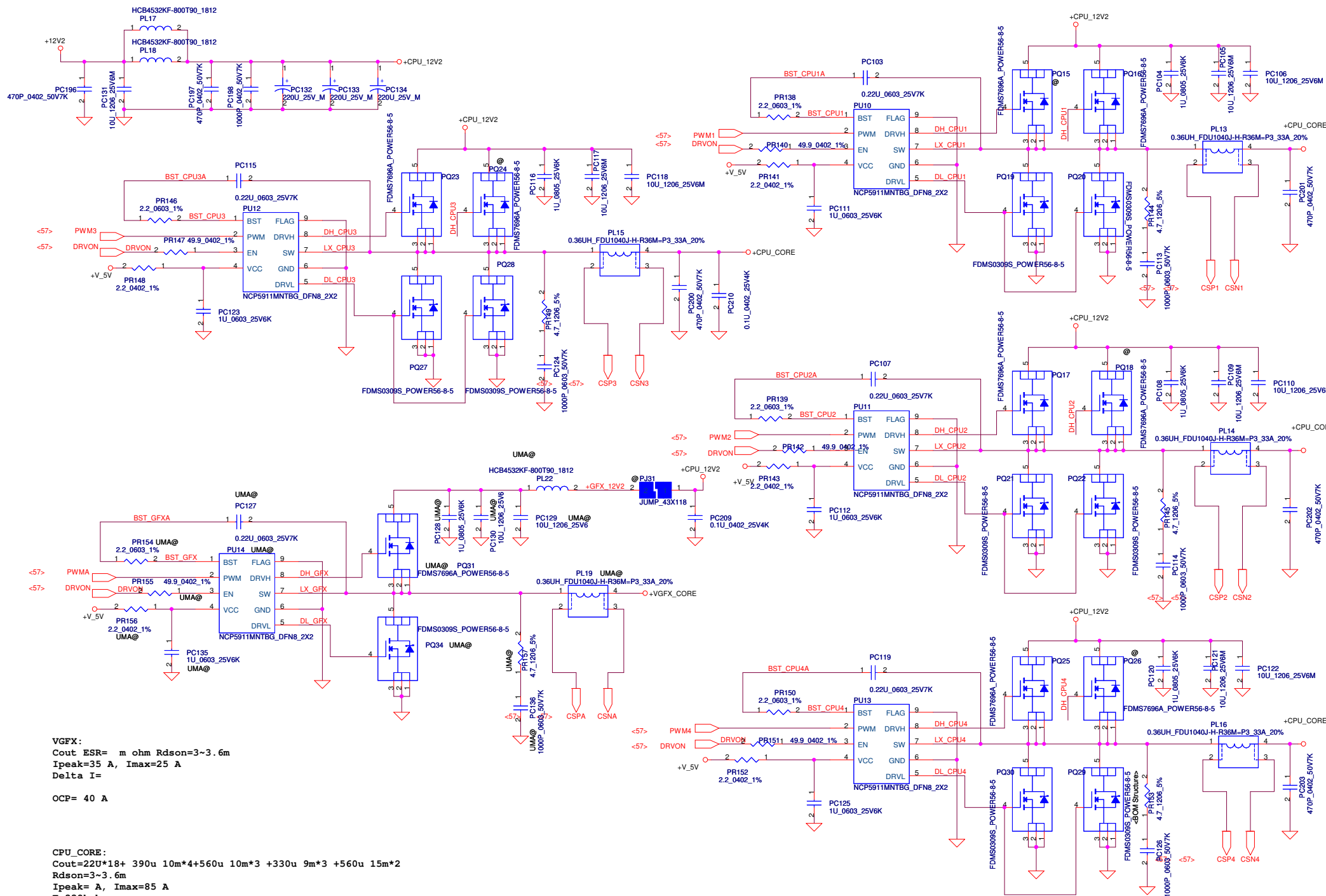
Default



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VGFX:
 $C_{out} ESR = m \text{ ohm}$ $R_{dson} = 3 \sim 3.6m$
 $I_{peak} = 35 \text{ A}$, $I_{max} = 25 \text{ A}$
 $\Delta I =$
 $OCP = 40 \text{ A}$

CPU_CORE:
 $C_{out} = 220u \cdot 18 + 390u \cdot 10m \cdot 4 + 560u \cdot 10m \cdot 3 + 330u \cdot 9m \cdot 3 + 560u \cdot 15m \cdot 2$
 $R_{dson} = 3 \sim 3.6m$
 $I_{peak} = \text{A}$, $I_{max} = 85 \text{ A}$
 $F = 338k \text{ hz}$
 $\Delta I =$

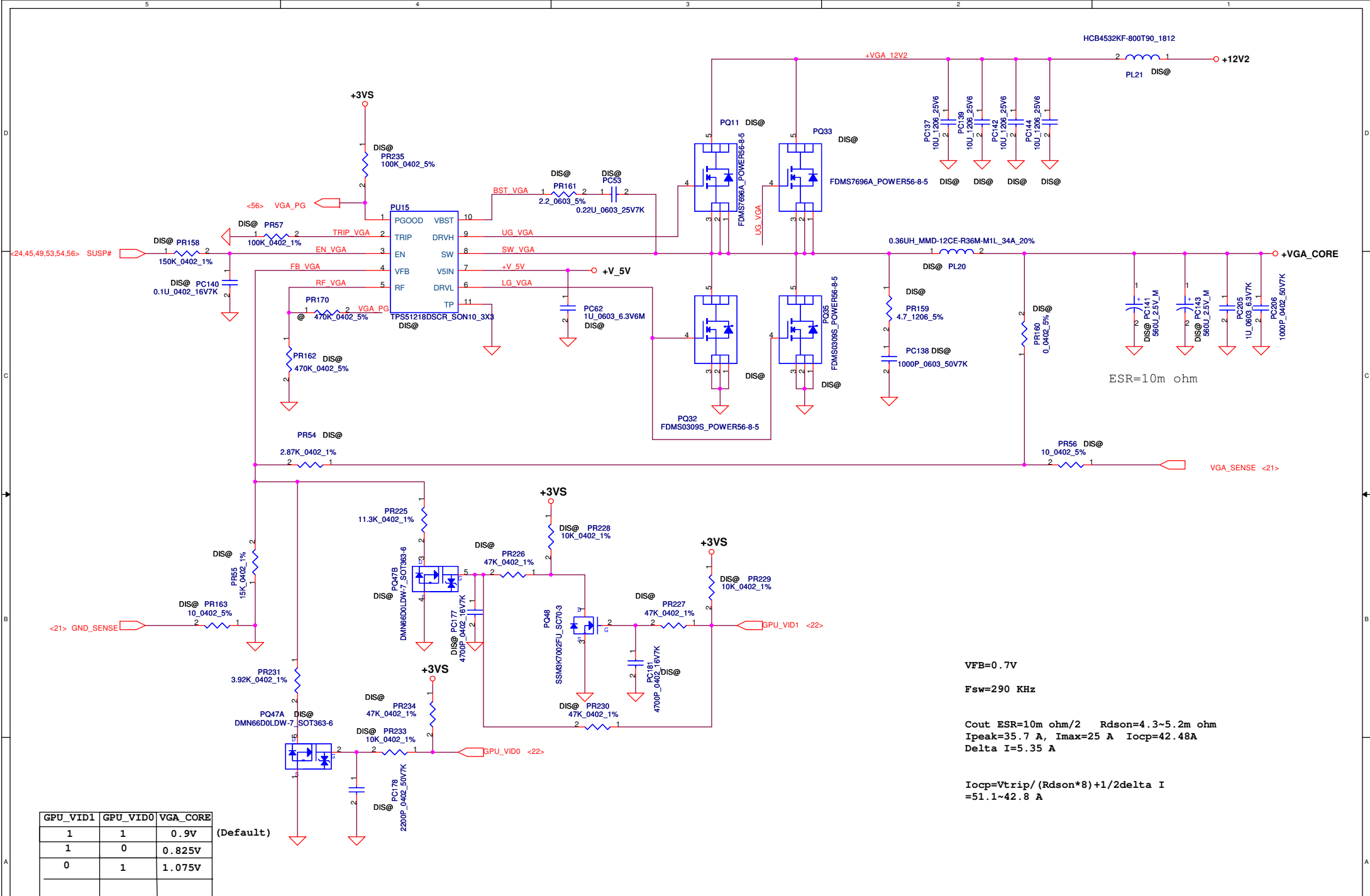
OCP= 135 A

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GPU_VID1	GPU_VID0	VGA_CORE
1	1	0.9V
1	0	0.825V
0	1	1.075V

(Default)

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Title			<Title>
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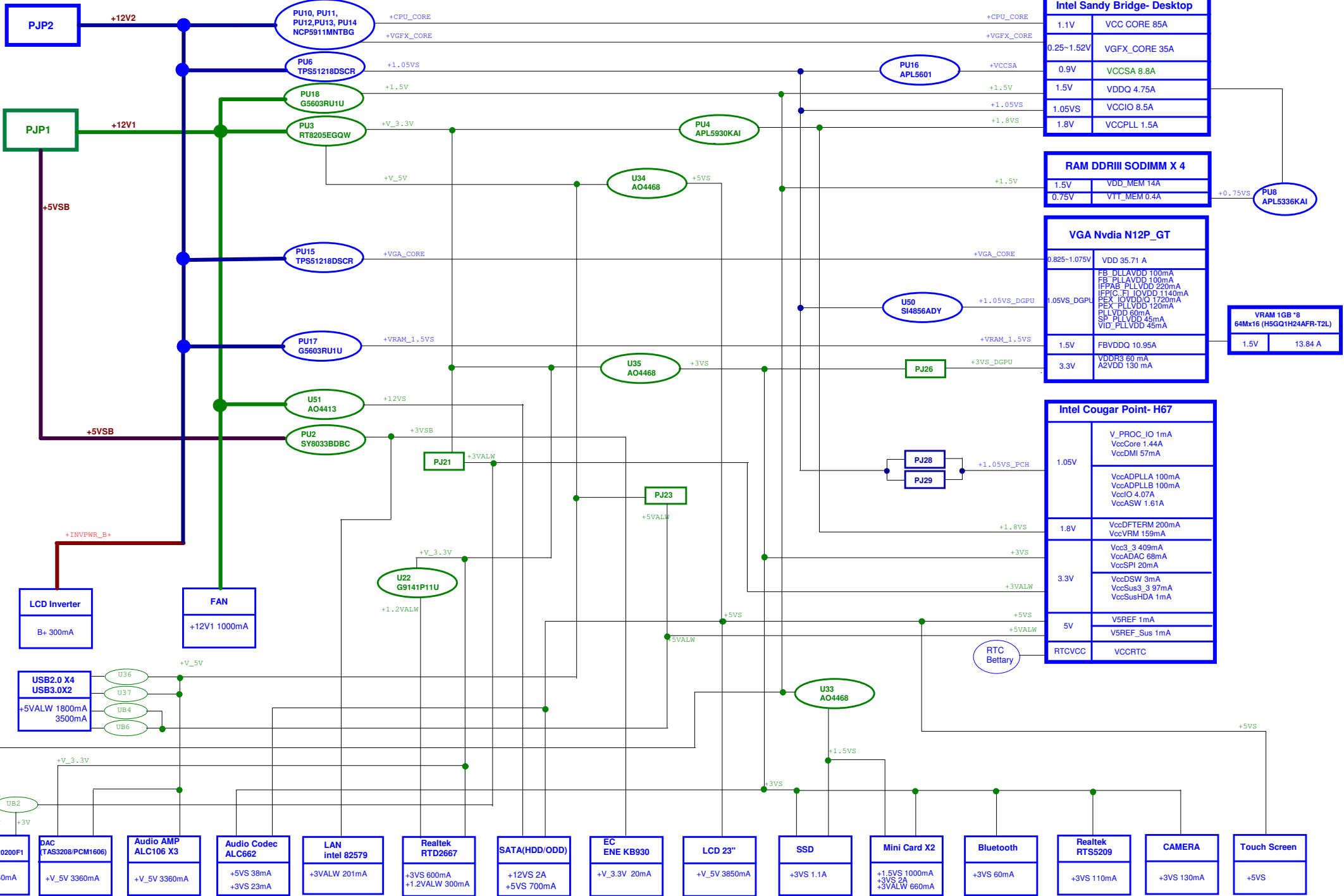
5

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Intel Sandy Bridge- Desktop	
1.1V	VCC CORE 85A
0.25~1.52V	VGFX_CORE 35A
0.9V	VCCSA 8.8A
1.5V	VDDQ 4.75A
1.05VS	VCCIO 8.5A
1.8V	VCCPLL 1.5A

RAM DDRIII SODIMM X 4	
1.5V	VDD_MEM 14A
0.75V	VTT_MEM 0.4A

VGA Nvidia N12P_GT	
0.825~1.075V	VDD 35.71 A
	FB DLLAVDD 100mA FB PLLAVDD 100mA IFPAB PLLVDD 220mA IFPAB PLLVDD 1140mA PEX IOVDDQ 1720mA PLLVDD 60mA SP PLLVDD 45mA VID PLLVDD 45mA
1.05VS_DGPU	
1.5V	FBVDDQ 10.95A
3.3V	VDDR3 60 mA A2VDD 130 mA

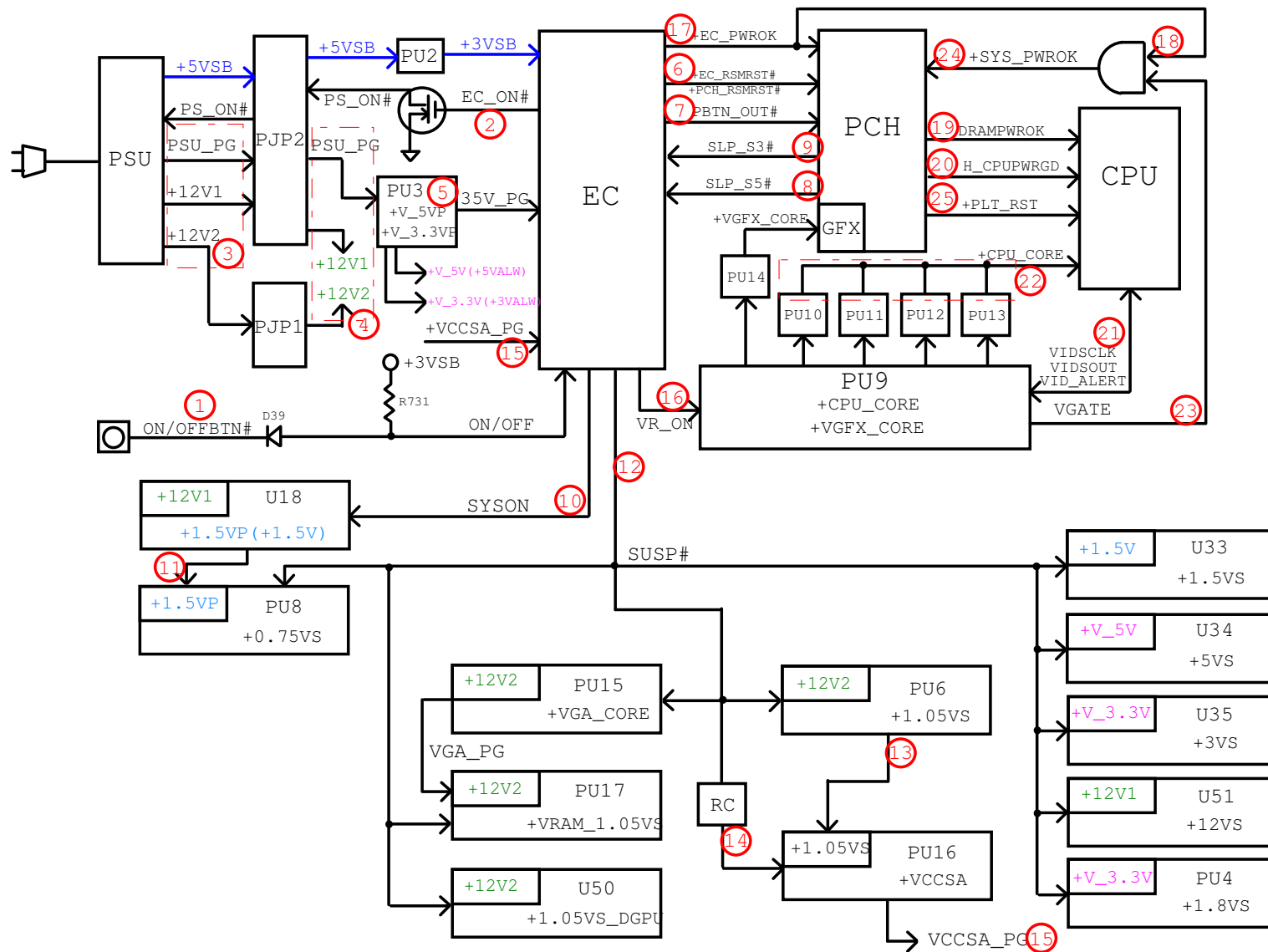
VRAM 1GB *3 64Mx16 (H5GQ1H24AFR-T2L)	
1.5V	13.84 A

Intel Cougar Point- H67	
1.05V	V_PROC_IO 1mA VccCore 1.44A VccDMI 57mA VccADPLLA 100mA VccADPLLB 100mA VccIO 4.07A VccASW 1.61A
1.8V	VccDFTERM 200mA VccVRM 159mA
3.3V	Vcc3_3 409mA VccADAC 68mA VccSPI 20mA VccDSW 3mA VccSus3_3 97mA VccSusHDA 1mA
5V	V5REF 1mA V5REF_Sus 1mA
RTCVC	VCCRTC

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MODEL NAME: PLA00 Power Sequence Block Diagram (Discrete)
PCB NAME: LA6951P
REVISION: 0.3
DATE: 2010/10/26



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